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# High bandwidth low power operational amplifier design and compensation techniques

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**High bandwidth low power operational amplifier design  
and compensation techniques**

by

Vaibhav Kumar

A thesis submitted to the graduate faculty  
in partial fulfillment of the requirements for the degree of  
MASTER OF SCIENCE

Major: Electrical Engineering

Program of Study Committee:  
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Ames, Iowa

2009

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## ABSTRACT

The need for high bandwidth operational amplifiers (op amp) exists for numerous applications. This need requires research in the area of Op Amp bandwidth extension. The exploited method in this thesis uses a class of compensation called *Indirect Feedback Frequency Compensation* in which the compensation current is fed back indirectly from the output to an internal high impedance node, to extend the bandwidth of an Op Amp.

Among various compensation methods for operational amplifiers, indirect compensation offers potentially large benefits in regards to power to speed trade-off. The indirect compensated Op Amps can exhibit significant improvements in speed over traditional Miller compensated Op Amps and result in much smaller layout size and lower power consumption. However the technique has not been widely used in practice due to a lack of clear design procedure. This thesis develops an analytical description of how indirect compensation works and derives key trade off equations among various specifications. These results provide the insight needed for practically designing operational amplifiers with this technique. Based on the results, a step-by-step design procedure is proposed for an operational amplifier using indirect compensation. To demonstrate the proposed design procedure, a two stage Op Amp is designed. The Op Amp achieved a 2 MHz gain-bandwidth product (GBW) driving a large capacitive load (100 pF). The GBW of the Op Amp was improved by a factor of 10 times compared to the miller compensation scheme. The amplifier documented in this thesis achieved a higher simulated figures-of-merit (FoMs) compared to the state-of-art and can be directly used in integrated systems to achieve higher performance.

## CHAPTER 1. INTRODUCTION

### 1.1 Background

Operational Amplifiers (Op Amps) are an integral part in design of various analog and mixed-signal systems. Their applications extend from dc bias applications to high speed ADC/DAC's and filters. General purpose Op Amps find their use in most analog subsystems, particularly in switched capacitor applications. In most of such systems, the overall system performance is strongly influenced by the Op Amp performance. With major enhancements in computer aided design (CAD) tools, advancements in semiconductor characterization and modeling, transistor scaling, and the progress of fabrication processes, the integrated circuit field is expanding rapidly. Integrated circuits once served the role of subsystem components, partitioned at analog-digital boundaries, however they now integrate complete systems on a chip by combining both analog and digital functions [2]. Complementary metal-oxide semiconductor (CMOS) technology has been the main-stay in mixed-signal because it provides density and power savings on the digital side, and a good mix of components for analog design. However, continued scaling of CMOS processes has continually challenged the established paradigm for operational amplifiers design. Scaling down of CMOS feature sizes enable yet faster speeds, the supply voltage is scaled down to enhance device reliability and improve power consumption. The expression for a short channel MOSFET transition frequency ( $f_T$ ) and open-loop gain ( $g_m \cdot r_o$ ) are given as [3]

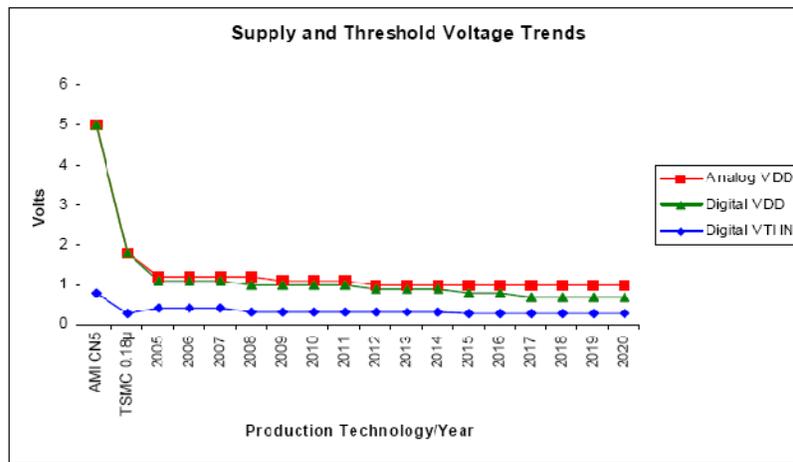
$$f_T \propto \frac{V_{EB}}{L} \quad \text{Equation 1.1}$$

$$g_m r_o \propto \frac{L}{V_{EB}} \quad \text{Equation 1.2}$$

where  $V_{EB}$ ,  $L$ ,  $g_m$  and  $r_o$  are the excess bias voltage, channel length, transconductance and output impedance respectively for a MOSFET.

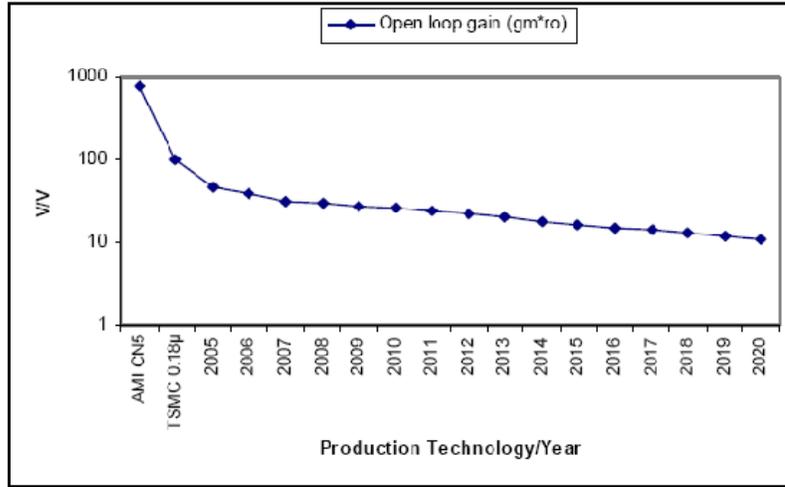
As can be seen from Equations 1.1 and 1.2, scaling down of feature sizes results in a higher  $f_T$ , and therefore faster operating transistors. However, this is achieved at the cost of a reduction in transistor's open loop gain. Thus, amplifiers designed in smaller feature size processes exhibit larger bandwidths but lower open loop gain.

Moving to lower feature size processes also requires reduced supply voltages. However, the threshold voltage of a transistor is not reduced by the same ratio in order to keep leakage currents under control. A direct result of this is the difficulty in using cascoding (vertical stacking of transistor to increase gain) transistors and other cascode based gain enhancement topologies.



**Figure 1-1 Supply voltage (Vdd) and threshold voltage (Vth) trends in future CMOS semiconductor processes technology (ITRS) [1]**

From Figure 1-1 it can be observed the upcoming process technologies in the future have continuous scaling down of analog VDD. However the threshold voltage is not scaling down with the same factor [1]. Also the scaling down of digital VDD is more aggressive in comparison to analog, which indicates the future holds even more challenge in integration of analog and digital designs.

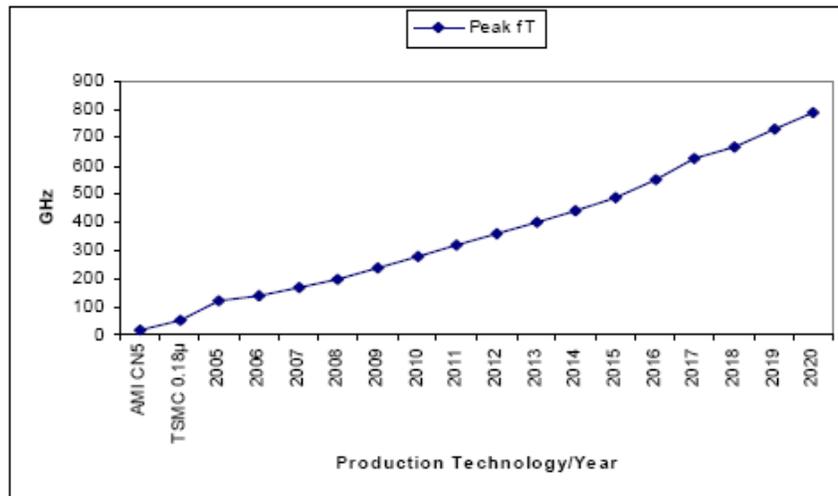


**Figure 1-2 Open loop gain trends in future CMOS process [1]**

Figure 1-2 highlights the projection of open-loop voltage gain drops from CMOS transistors. The open loop gain for sub-micron processes currently is at the order of 10's which already poses significant design challenges. Furthermore, the future processes are not showing promising transistor matching data as the feature sizes reduce. Equation 1.3 gives the expression for threshold voltage mismatch ( $\sigma_{th}$ ) given by[1]

$$\sigma_{th} \propto \sqrt{\frac{1}{L \cdot W}}$$

**Equation 1.3**



**Figure 1-3 Transistor transition frequency ( $f_T$ ) trends in future CMOS processes [1]**

Figure 1-3 shows the trends in transistor transition frequency ( $f_T$ ) with CMOS process technology progression.

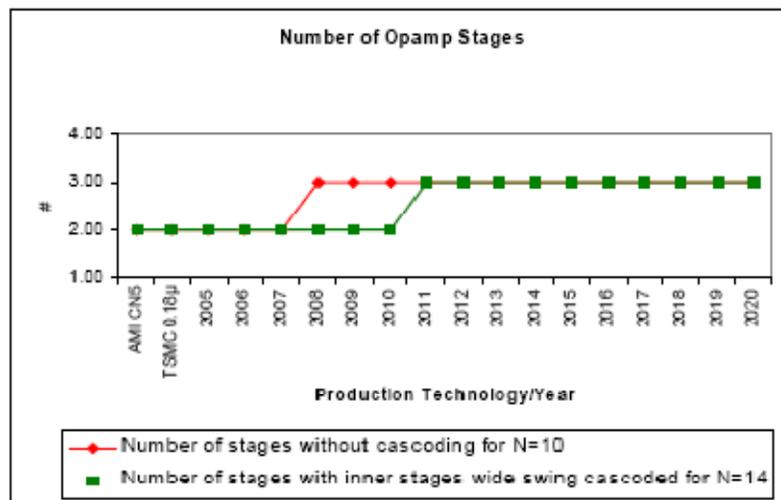
From the above trends it is evident that designing a high gain operational amplifier in future CMOS processes is a challenging task. Now, for an N bit resolution ADC, the open loop dc gain ( $A_{DC}$ ) requirement is expressed as [4]

$$|A_{DC}| \geq \frac{1}{\beta} \cdot 2^{N+1} \quad \text{Equation 1.4}$$

where  $\beta$  is the feedback factor in the Op Amp architecture. For  $\beta = \frac{1}{2}$ , which is the case in a R-2R data converter and other various architectures the required open loop is given as [4]

$$|A_{DC}| \geq 2^{N+2} \quad \text{Equation 1.5}$$

Therefore for a 10 and 14 bit resolution ADC, the open loop dc gain required from the Op Amp would be 4K and 16K respectively. Figure 1-4 illustrated the number of amplifier stages inside an Op Amp required to achieve sufficient Op Amp gain for 10 bit



**Figure 1-4** Number of stages required to achieve the DC gain requirement for 10 and 14 bit resolution settling. The figure shows number of cascaded stages required with employing any cascoding for 10 bit ADC settling. It also shown the number internal stages with wide swing cascoded stage required for a 14 bit resolution settling [1]

settling requirements. It also depicts the number of internal stages required with wide swing cascoded structures to achieve sufficient gain for 14 bit settling requirements. The swing for a wide swing cascode is given as  $(2V_{DS,sat}, V_{DD}-2V_{DS,sat})$ , where  $V_{DS,sat}$  is the saturation voltage for the transistor for a given bias [5]. With  $V_{DS,sat}$  not reducing in the same fashion as the power supplies, it would become even more difficult to use a wide swing cascode itself.

Figure 1-4 also depicts the needs and trends of future Op Amps architectures. It predicts that stepping into the next decade operational amplifiers with more than two stages would be needed to recover the dc gain. Also with the emerging low voltage, low power applications markets, such as cell phones and portable media devices, the required open-loop dc gain can only be achieved by Op Amp with more than two stages.

Applications of high gain operational amplifiers with more than two stages can be extended to comparators, sigma delta A/D, low distortion oscillators, multivibrators, and a host of others. This thesis presents development of novel high-speed, low voltage, low-power, multi-stage Op Amp topologies which tremendously improve upon the state-of-art. Also the improved Op Amp frequency compensation scheme, called indirect feedback compensation introduced in [6] is amply developed and presented. The indirect feedback compensation, when applied to multi-stage Op Amp design, solves many problems with techniques proposed in literature, and enables realization of extremely low-power Op Amp topologies.

## 1.2 Thesis Outline

The research presented in this thesis covers studies related to frequency compensation methods of operational amplifiers and low voltage low power analog circuit design. Each chapter presents the analysis of the problem and the development of the solution. A brief outline of each chapter is described below.

Chapter 2 covers the general background information for frequency compensation. The basics of feedback network theory and stability associated with negative feedback amplifiers are discussed. Basic frequency compensation techniques such as miller compensation are discussed and the limitations are analyzed. Novel and more recent techniques promising high performance are also discussed.

Chapter 3 covers the analysis and development of the indirect feedback compensation strategy. An exact analysis of the strategy and a simplified analytical model for indirectly compensated Op Amps are presented. The potentials for the architecture are discussed and a design procedure is provided.

Chapter 4 illustrates the application of the indirect feedback compensation. A two stage amplifier employing indirect feedback compensation is designed. The frequency compensation is then employed in traditional cascoded architecture to demonstrate the feasibility of the frequency compensation technique.

Chapter 5 provides the conclusions drawn from the work presented in this thesis along with the directions for future research on this topic.

## CHAPTER 2. LITERATURE REVIEW OF FREQUENCY COMPENSATION TECHNIQUES

### 2.1 Introduction

Feedback is a powerful technique that finds wide application in analog circuits. The high gain from amplifiers ensures the closed loop transfer characteristics with negative feedback are independent of the Op Amp gain. However, an adequate gain is a key requirement to utilize this technique.

### 2.2 Feedback Circuit Theory

Figure 2-1 shows a general negative feedback system [7], where  $H(s)$  and  $G(s)$  are called the feedforward and the feedback networks, respectively. Since the output of  $G(s)$  is equal to  $G(s)Y(s)$ , the input to  $H(s)$ , called the feedback error and output are given by

$$E(s) = X(s) - G(s)Y(s) \quad \text{Equation 2.1}$$

$$Y(s) = H(s)[X(s) - G(s)Y(s)] \quad \text{Equation 2.2}$$

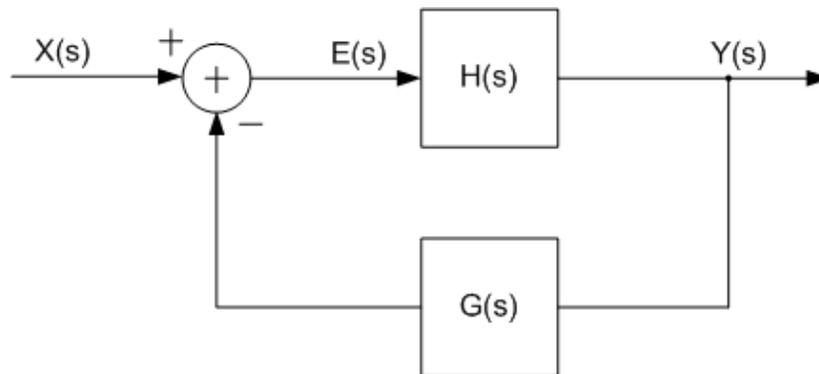


Figure 2-1 General negative feedback system

Thus

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 + G(s)H(s)} \quad \text{Equation 2.3}$$

The quantity  $H(s)$  is the open loop transfer function and  $Y(s)/X(s)$  is the closed loop transfer function.  $H(s)$  represents the operational amplifier and  $G(s)$  is a frequency independent quantity. In other words, a fraction of the out signal is sensed and compared with the input and generating an error term. In negative feedback system, the error term is minimized, thereby making the output of  $G(s)$  an accurate copy of the input and hence the output of the system is an accurate replica of the input [7].

Feedback circuits provide gain desensitization, i.e. the closed loop gain is much less sensitive to the open loop gain [5]. This property can be quantified as following

$$\frac{Y}{X} = \frac{A}{1 + A\beta} \approx \frac{1}{\beta} \left(1 - \frac{1}{A\beta}\right) \quad \text{Equation 2.4}$$

where  $A$  and  $\beta$  are the low frequency gain of  $H(s)$  and  $G(s)$  respectively, and the dc gain  $A\beta \gg 1$ . It can be noted that the closed-loop gain is determined, to the first order by the feedback factor,  $\beta$ . More importantly, even if the open-loop gain,  $A$ , varies by a factor of 2,  $Y/X$  varies by a small percentage because  $1/(A\beta) \ll 1$ . The quantity  $A\beta$  is called the loop gain. The loop gain plays an important role in feedback system. As seen from Equation 2.4 that the higher  $A\beta$  is, the less sensitive  $Y/X$  will be to the variation in  $A$ . From another perspective, the accuracy of the closed-loop gain improves as the open loop gain or feedback factor are maximized. However, as the feedback factor  $\beta$  is increased, the closed loop gain decreases  $Y/X \approx 1/\beta$ , so there is an inherent trade-off between precision and the closed loop gain.

Negative feedback also exhibit effects on the bandwidth of the amplifier. Certain configurations of a feedback amplifier extend the closed bandwidth of the amplifier beyond the open loop amplifier. Assuming the feedforward amplifier in Figure 2-1 has a single transfer function as given below

$$H(s) = \frac{A_0}{1 + s\omega_0} \quad \text{Equation 2.5}$$

where  $A_0$  denotes the low frequency gain and  $\omega_0$  is the 3-dB bandwidth. The transfer function of the closed loop system can then be expressed as

$$\frac{Y}{X}(s) = \frac{\frac{A_0}{1 + \frac{s}{\omega_0}}}{1 + \frac{\beta A_0}{1 + \frac{s}{\omega_0}}} = \frac{\frac{A_0}{1 + \beta A_0}}{1 + \frac{s}{(1 + \beta A_0)\omega_0}} \quad \text{Equation 2.6}$$

The numerator in Equation 2.6 is the closed loop low frequency gain equivalent Equation 2.4. The denominator provides the location of the pole at  $(1 + \beta A_0)\omega_0$ . Comparing this to Equation 2.5 the 3-dB bandwidth has increased by a factor of  $(1 + \beta A_0)$ . The extended bandwidth comes at the cost of proportional reduction in the gain as the product of gain and bandwidth is a constant for such an operational amplifier.

Another very important property of negative feedback is the suppression of nonlinearity in analog circuits [8]. Nonlinearity can be regarded as the variation of the small signal gain with the input dc level. Negative feedback keeps the overall closed loop gain nearly constant and almost independent of the amplifier open loop gain. Therefore negative feedback circuits reduce distortion resulting from the change in the slope of the amplifier transfer curve. Mathematical analysis of the effect of a feedback system on nonlinearity of a circuit is very complex and can be found in [3, 5].

## 2.3 Stability of Feedback Systems

Negative feedback finds diverse application in processing of analog signals. The properties of feedback described in section 2.2 allow precise operations by suppressing variations of the open loop characteristics. However, feedback systems suffer from potential instability, that is, they may oscillate.

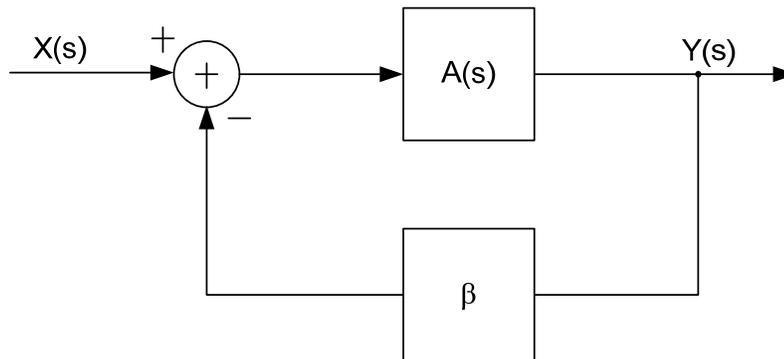


Figure 2-2 Basic negative feedback system

Considering the negative feedback system shown in Figure 2-2 the closed loop transfer function can be written as

$$\frac{Y}{X}(s) = \frac{H(s)}{1 + \beta H(s)} \quad \text{Equation 2.6}$$

If  $\beta H(s = j\omega_1) = -1$ , then from observing Equation 2.6 the gain goes to infinity and the circuit starts to amplify its own noise until it eventually begins to oscillate. This condition can be expressed as

$$|\beta H(j\omega_1)| = 1 \quad \text{Equation 2.7}$$

$$\angle \beta H(j\omega_1) = 180^\circ \quad \text{Equation 2.8}$$

which are called the ‘‘Barkhausen’s Criteria’’. It can be observed that the total phase shift around the loop at  $\omega_1$  is  $360^\circ$  because the negative feedback introduces itself a  $180^\circ$  of phase shift. The  $360^\circ$  of phase shift is required for oscillation as the noise has to shift by  $180^\circ$

to be in phase with the signal to add. The other condition on loop gain being unity or greater is required to enable the growth of the oscillation amplitude.

The condition necessary and sufficient for negative feedback stability is that all the poles of the feedback system are have a negative and real part. This from Laplace's criteria translates to the poles being on the left half side of the plane. It may be difficult to analyze the stability of a complex system from looking at the closed loop poles of the system, since finding the zeros of the denominator  $1+\beta A(s)$  may be complicated. It would be therefore much useful if the closed loop stability could be predicted from observing the open loop response of the amplifier.

The concept of phase margin for an open loop amplifier is good indicator of the stability of the closed loop system. From the Nyquist criterion "If  $|A(j\omega)| > 1$  at the frequency where  $\text{ph } A(j\omega) = -180^\circ$ , then the amplifier is unstable." Figure 2-3 shows the loop gain magnitude  $|A(j\omega)|$  is unity at frequency  $\omega_0$ . At this frequency the phase of  $A(j\omega)$  has not reached  $-180^\circ$  for the case shown, and using the Nyquist criterion state we conclude that this feedback loop is stable.

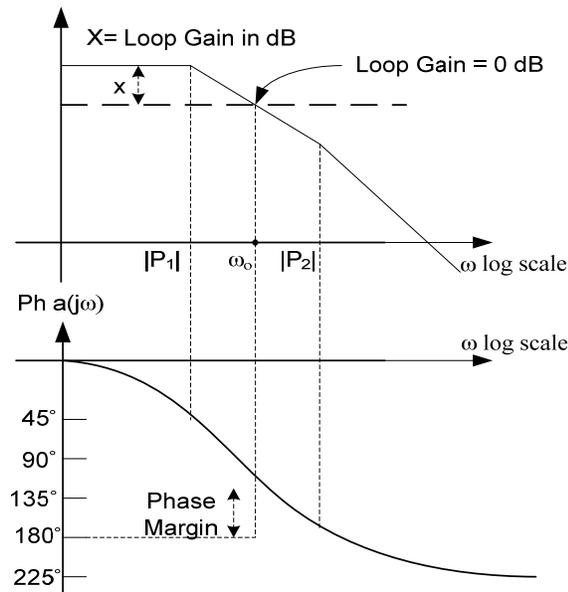


Figure 2-3 Amplifier gain and phase versus frequency showing the phase margin

As  $|A(j\omega)|$  is made closer to unity at the frequency where  $\text{ph } |A(j\omega)| = -180^\circ$ , the amplifier has a smaller margin of stability, and this can be specified in two ways [9]. The most common is the phase margin, which is defined as follows:

Phase margin =  $180^\circ + (\text{ph } A(j\omega) \text{ at frequency where } |A(j\omega)| = 1)$ . The phase margin is indicated in Figure 2-3 and must be greater than  $0^\circ$  for stability. [3]

## 2.4 Basic Frequency Compensation Techniques of Operational Amplifier

The single stage amplifiers are inherently stable and typically have excellent frequency response assuming the gain bandwidth is ten times higher than the single pole. However, single stage amplifiers suffer from low dc gain and is even less for submicron CMOS transistors. In general, Op Amps require at least two gain stages which introduce multiple poles in the frequency response. The poles contribute to the negative phase shift and may cause  $\angle FA$  to reach  $-180^\circ$  before the unity gain frequency. Therefore due to insufficient phase margin the circuit would oscillate. Thus the amplifier circuit needs to be modified to increase the phase margin and stabilize the closed loop circuit. This process is called “compensation”. By intuition, two different approaches may be taken to stabilize the loop. The more straightforward approach way is make the gain drop faster in order for the phase shift to be less than  $-180^\circ$  at the unity gain frequency. This approach achieves stability by reducing the bandwidth of the amplifier and the most popular pole splitting method uses this procedure. Another compensation method pushes the phase crossover frequency out by decreasing the total phase shift. In this particular case the total number of poles needs to be reduced while still maintaining the dc gain. This is achieved by introducing zeros into the open and close loop transfer function to cancel the poles, or using feedforward paths to improve the phase margin without narrow-banding the bandwidth as much as the pole splitting does.

### 2.4.1 Parallel Compensation

Parallel compensation is a classical way to compensate the Op Amp. A capacitor is connected in parallel to the output resistance of a gain stage of the operational amplifier to modify the pole. It is not commonly used in the integrated circuit due to the large capacitance value required to compensate the Op amp, which considerable die area.

### 2.4.2 Pole Splitting – Single Miller Compensation (SMC)

The most widely used compensation technique in analog circuit and systems design is undoubtedly pole splitting. A miller capacitor is used to split the poles, which causes the dominant pole to move to a much lower frequency and thus reducing the bandwidth and providing ample stability. This method is featured in the original 741/101 bipolar Op Amps designed by Robert Widlar and was widely implemented henceforth [10].

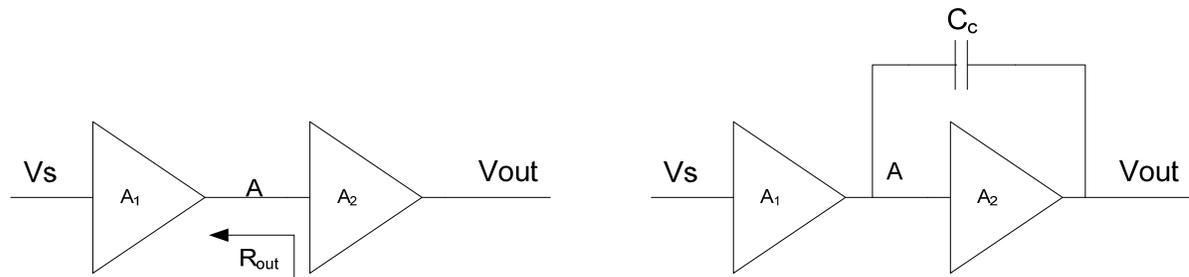


Figure 2-4 Miller compensation of a two-stage Op amp

Figure 2-4 shows the block diagram of a two-stage operational amplifier employing *Miller Compensation* or Direct compensation technique. The Op Amp consists of an input differential pair stage with gain  $A_1$ . The second stage (output stage) is biased from the output of the differential stage and driving a large capacitive load.

Before the compensation, the poles of the two stage cascade are given as  $p_1 = \frac{1}{R_1 C_1}$  and  $p_2 = \frac{1}{R_2 C_2}$ , where  $R_k$  and  $C_k$  are the resistance and capacitances at those nodes. In order to

achieve dominant pole stabilization of the Op amp, Miller compensation is used to perform pole splitting. A compensation capacitor is placed between the output of the amplifier and the output of the first stage as shown Figure 2-4. The compensation capacitor seen at node A is then  $(1+A_2)C_c$  due to the miller effect [8]. This kind of compensation splits the two pole apart as shown in Figure 2-6. The dominant pole is moved to a much lower frequency, thereby reducing the bandwidth, while the non-dominant pole is moved to a higher frequency. However the miller capacitor also introduces a right half plane zero due to the feedforward current from the output of the internal stage to output of the amplifier. Figure 2-5 shows the small signal model

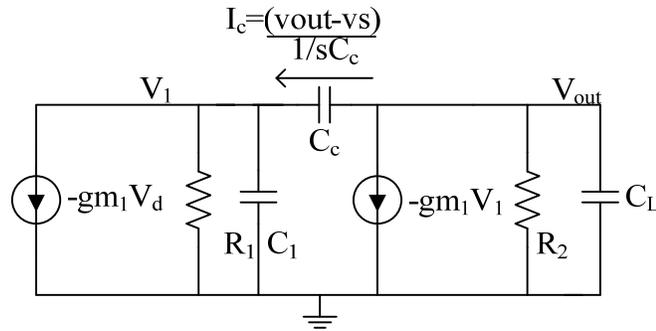


Figure 2-5 Small signal mode for two stage amplifier with miller compensation

The small signal transfer function for the two stage amplifier with miller compensation is given as

$$\frac{V_{out}}{V_d} = \frac{gm_1 R_1 gm_2 R_2 \left(1 - \frac{s}{z_1}\right)}{\left(1 - \frac{s}{p_1}\right) \left(1 - \frac{s}{p_2}\right)} \quad \text{Equation 2. 9}$$

The RHP zero is located at

$$z_1 = \frac{gm_2}{C_c} \quad \text{Equation 2. 10}$$

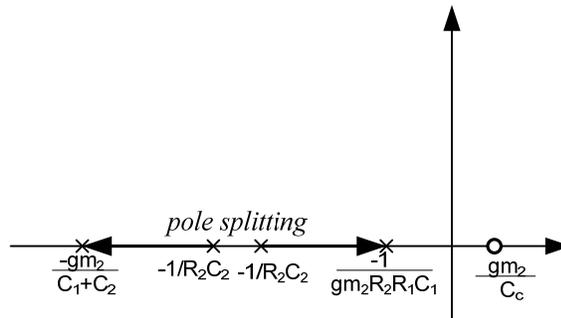
The dominant pole is located at

$$p_1 = -\frac{1}{gm_2 R_2 R_1 C_c} \quad \text{Equation 2. 11}$$

The non dominant pole is locate at

$$p_2 = -\frac{gm_2 C_c}{C_c C_1 + C_1 C_L + C_c C_L} \approx -\frac{gm_2}{C_1 + C_L} \quad \text{Equation 2. 12}$$

The overall dc gain of the amplifier from Equation 2.9 is  $gm_1 R_1 gm_2 R_2$ , and the unity gain frequency for the amplifier is  $f_{un} = gm_1/2\pi C_c$ . The pole splitting due to the miller compensation is shown below in Figure 2-6.



**Figure 2-6 New location of poles due to miller compensation**

Figure 2-7 shows the frequency response of the Miller compensated two-stage amplifier. It can be observed that the RHP zero degrades the phase response of the open loop amplifier. The phase contribution due to the RHP zero is  $-\tan^{-1}\left(\frac{f}{f_{z1}}\right)$  which leads to instability when the second pole moves closer to the unity gain frequency ( $f_{uf}$ ). In Figure 2-7 the RHP zero not only flattens the magnitude response due to the dominant pole but also degrades the phase make it difficult to stabilize the amplifier. This RHP zero can be eliminated by blocking the feed-forward compensation current, while allowing the feed-back component of the compensation current achieve pole splitting [11]. Several methods have been suggested in [5] and [12] to cancel the RHP zero which will be discussed in the next section.

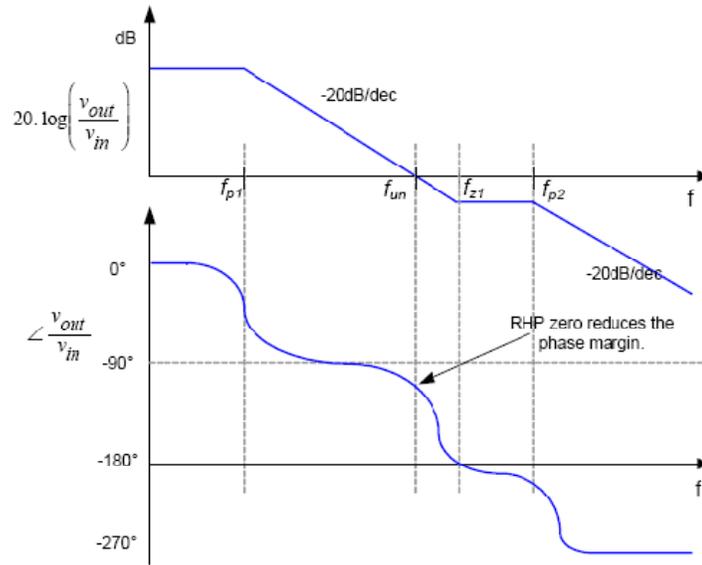


Figure 2-7 Effect of RHP zero on the frequency response of two stage amplifier

### 2.4.3 Miller compensation with Zero Nulling Resistor

A common method to cancel the RHP zero is by using a series resistor with compensation capacitor as shown in Figure 2-8. With the addition of series resistor [13], the new location of the zero is

$$z_1 = \frac{1}{\left(\frac{1}{gm_2} - R_z\right) C_c} \quad \text{Equation 2. 13}$$

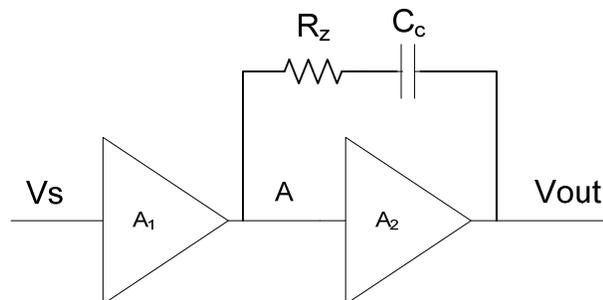


Figure 2-8 Miller compensation with series resistor

Observing Equation 2.13 the location of zero can be controlled with the value of the series resistor  $R_z$ . For  $R_z=1/g_{m2}$  the zero moves to infinity and for  $R_z$  greater than  $1/g_{m2}$  the zero moves to the LHP and help improving the phase margin. This addition of the series resistor does not move the location of the  $p_1$  and  $p_2$ , however introduces a third pole at  $p_3 = \frac{1}{R_z C_1}$  which is far away from the other two poles. The resistor  $R_z$  can be implemented using a transistor in triode region, and can be made to track the value of  $1/g_{m2}$  and cancel the RHP zero.

#### 2.4.4 Other Multistage Operational Amplifier Compensation

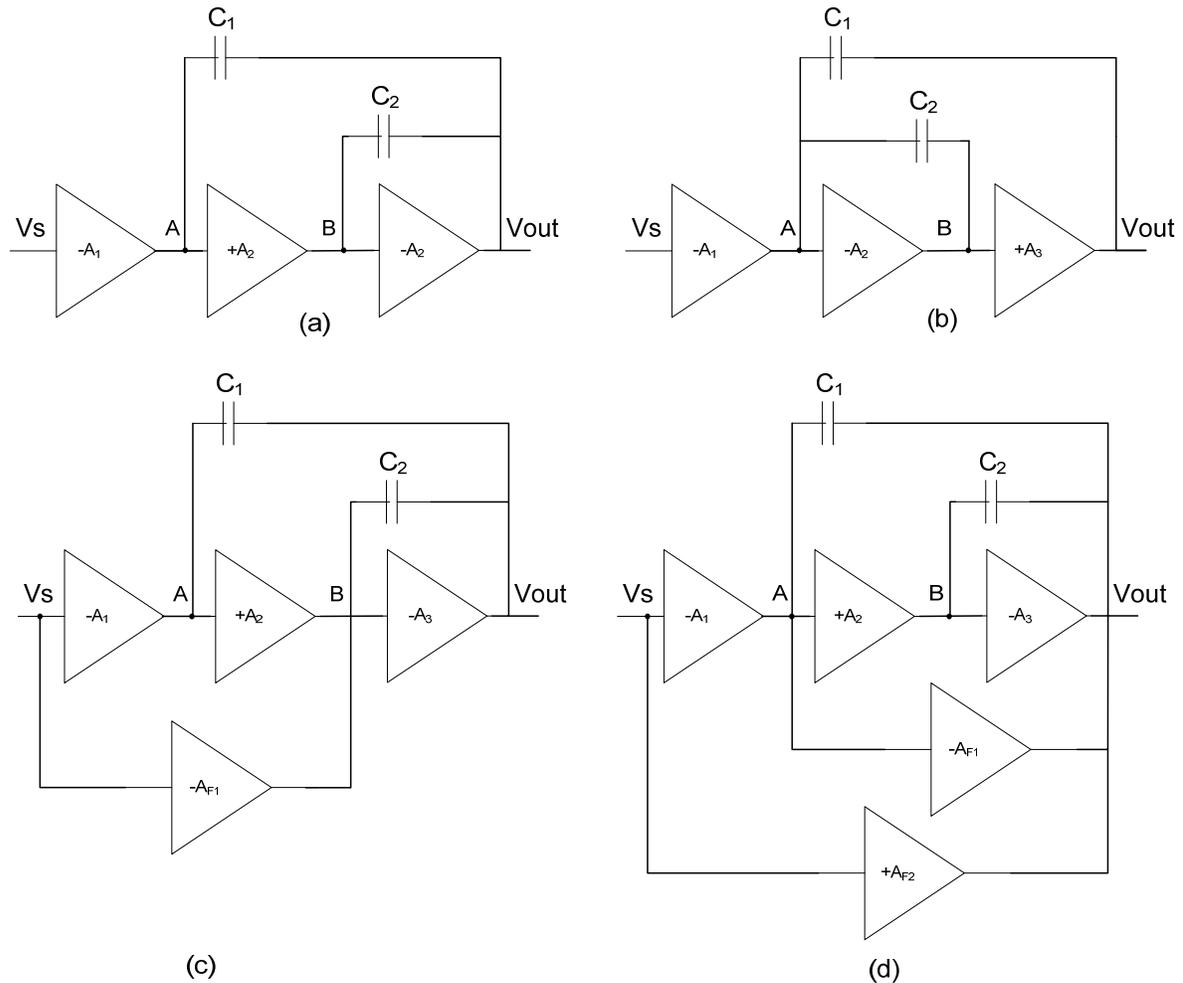
As discussed section 1, with supply voltages declining, the single-stage cascoded based architectures have become unsuitable for some applications because of the limited signal swing capability. As a result, designers have started looking for alternative architectures to overcome the drawbacks of single stage amplifiers. One alternative is to recover the gain by cascading stages. However, as observed in the previous section, cascaded structures are unstable in nature, and simple miller compensation technique analyzed in the previous section reduces the bandwidth of the amplifier significantly. In the recent times new architectures have been proposed to tackle this issue [14]. This section briefly describes the recent developments in the area and bring upfront the pros and cons of each architecture.

##### 2.4.4.1 Nested Miller Compensation (NMC) and the Variants

Multistage amplifiers have more poles and zeros compared to the single stage amplifier. Thus the frequency response of these multistage amplifiers is much more complex. As a result, multistage amplifiers suffer from closed loop stability issues. Frequency compensation attempts to stabilize the amplifier, but reduce the bandwidth of the amplifier significantly, thus amplifiers with more than 3 stages are hardly considered. Single Miller Compensation as described in previous section can be effectively used to stabilize two stage amplifiers. The concept can be extended to multistage amplifier by nesting the miller

compensation strategy. The technique is called Nested Miller Compensation (NMC) is described in [15-17] and is shown in Figure 2-9(a). There are certain drawbacks related to the NMC approach. A total of  $N-1$  capacitors are needed to stabilize an  $N$  stage amplifier. The necessity to drive the compensation capacitor along with the capacitive load requires the output stage to have a high transconductance to attain wide bandwidth and high slew rate.

To address the reduction in bandwidth many variants of the NMC have been proposed. Shown in Figure 2-9, Reverse nested miller compensation (RNMC) [18], Multipath nested miller compensation (MNMC) [16], Nested Gm-Cc compensation (NGCC) [19] are some of the alternatives to recover the bandwidth.



**Figure 2-9 (a) Nested Miller Compensation (NMC), (b) Reverse Nested Miller Compensation (RNMC), (c) Multipath Nested Miller Compensation (MNMC), (d) Nested Gm-Cc Compensation (NGCC)**

RNMC improves the bandwidth by making the second stage have a negative gain and the output stage having a positive gain [18]. This allows the miller capacitor  $C_2$  being wrapped around the second stage and thus avoid the loading of compensation capacitor on the output in comparison to NMC.

The variation between the NMC and MNMC is that the latter has a feedforward path which is also a high speed path. The feedforward path introduces a zero which can be used to cancel one of the non-dominant poles and extend the bandwidth. This significantly increases the complexity of the design and the extra path increases the power and chip area as well. Further pole-zero cancellation need to be accurate to exploit the benefits of the architecture. It has also been well documented about the poor transient response for a pole zero doublet [16].

The difference between NGCC and MNMC is that the idea of feedforward stage is replicated for each stage. The topology is much easier to analyze and understand as the transfer function is much simpler in comparison to MNMC.

The basic idea behind all of the above variants of NMC is to introduce a zero to cancel one of the non dominant poles. All these topologies however still rely in the miller capacitor to split the dominant and non dominant pole from the load capacitor. Thus the miller capacitor scales larger with increasing capacitive load drives. The next section address a new class of topology used for driving large capacitive loads and show potential for having bandwidth even larger than single stage.

#### **2.4.5 Active Feedback and Indirect Compensation**

A newer class of frequency compensation driving large loads was proposed in [13] and [14]. As shown in Figure 2-10(a), the technique is a variant of miller compensation between nodes B and node Vout. A form of indirect compensation is used here to feedback the compensation current from node Vout to node A. In the block diagram, the high gain

block (HGB) is the cascade of stages to achieve the high dc gain, while the high speed block (HSB) is to provide the high frequency response and stability. Another variation of indirect compensation is presented in [20] by Sansen. Figure 2-10(b) shows the Transconductance with Capacitance feedback frequency compensation (TCFC). Both architectures promise in providing stellar frequency response due to the reduction of miller capacitance size required by these topologies. Furthermore the compensation current for the internal amplifier is feedback internally from  $V_{out}$  to  $V_s$  in AFFC and in TCFC from  $V_{out}$  to node B. A generalized indirect feedback compensation scheme is proposed and analyzed in detail in this thesis. The compensation scheme enables in achieving very low-power low-voltage multistage Op Amps with improved stability.

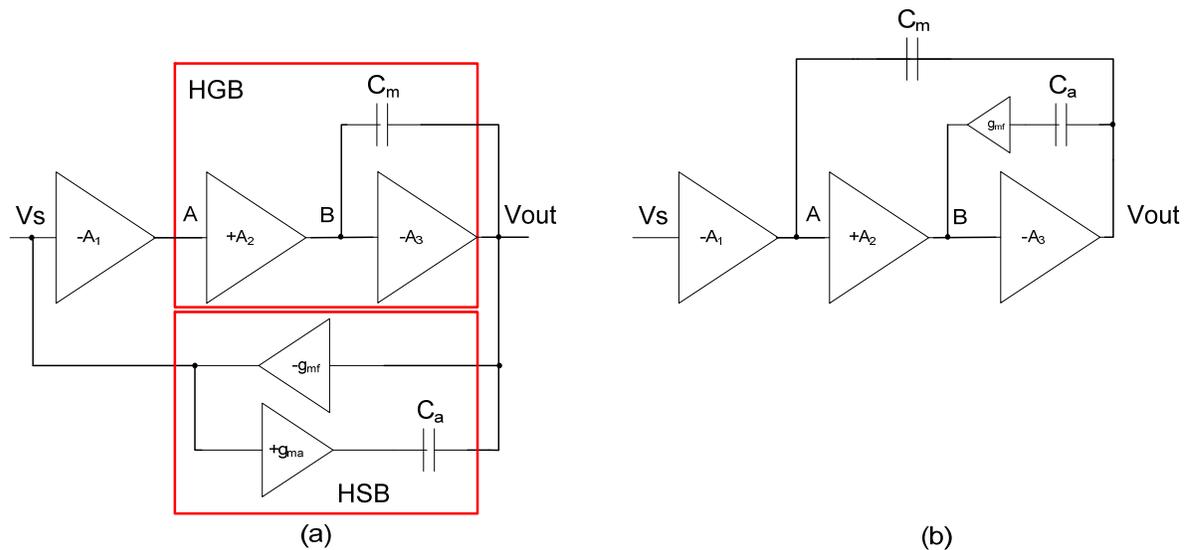


Figure 2-10 (a) Active feedback frequency compensation (AFFC), (b) Transconductance with capacitance feedback frequency compensation (TCFC)

## CHAPTER 3. INDIRECT FEEDBACK FREQUENCY COMPENSATION

### 3.1 Introduction

As introduced in the previous section, the class of compensation in which the compensation current is fed back indirectly from the output to the internal high impedance node is called *Indirect Feedback Frequency Compensation*. Here the compensation capacitor is connected from the output to an internal low impedance node, which indirectly feeds the current to the high impedance node A. Figure 3-1 depicts the block diagram of the Indirect Feedback Frequency Compensation. In the block diagram the effective low impedance attached at node A is detected by  $R_i$ .

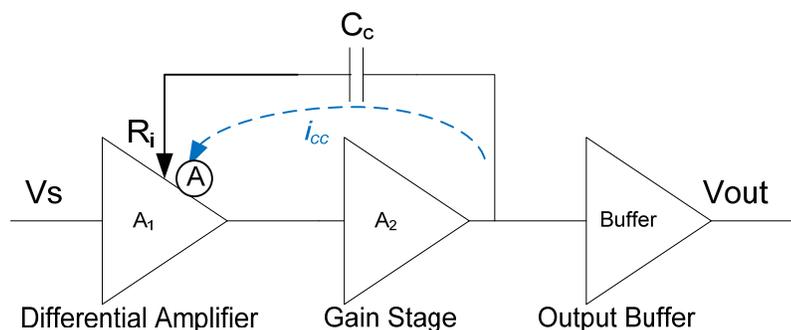


Figure 3-1 Block diagram depicting Indirect Feedback Frequency Compensation

### 3.2 Small Signal Analysis

In order to gain insight of the indirect feedback frequency compensation technique, a detailed analytical and mathematical analysis is required. Figure 3-2 shows the topology of the two stage Op Amp. A common gate amplifier M6 is used to provide the compensation current indirectly to the high impedance node  $V_1$ . The common gate amplifier isolated the node  $V_1$  from the compensation capacitor and thus does not load the out of the first stage.



$R_A$  and  $C_A$  represent the parasitics at the internal low impedance node  $V_A$ . The nodal analysis can be thus done as shown below:

$$-gm_1V_s + \frac{V_1}{R_1} + V_1sC_1 - gm_{cg}V_a + \frac{V_1 - V_a}{r_{oc}} = 0 \quad \text{Equation 3.1}$$

$$gm_5V_1 + \frac{V_{out}}{R_2} + V_{out}sC_L + sC_c(V_{out} - V_a) = 0 \quad \text{Equation 3.2}$$

$$\frac{V_A - V_1}{r_{oc}} + gm_{cg}V_a + V_AsC_A + \frac{V_A}{R_A} + sC_c(V_A - V_{out}) = 0 \quad \text{Equation 3.3}$$

On simultaneously solving the above three equation, the transfer function from  $V_{out}$  to  $V_d$  can be expressed as

$$\frac{V_{out}}{V_s} = -A_V \left( \frac{b_0 + b_1s}{a_0 + a_1s + a_2s^2 + a_3s^3} \right) \quad \text{Equation 3.4}$$

The third order transfer function has three poles and single left half plane zero. The exact values of the coefficients are given below:

$$A_v = gm_1R_1gm_5R_2 \quad \text{Equation 3.5}$$

$$b_0 = (1 + gm_cRA)r_{oc} + RA \quad \text{Equation 3.6}$$

$$b_1 = RA \left[ r_{oc}(C_c + C_A) + gm_cr_{oc} - \frac{C_c}{gm_5} \right] \quad \text{Equation 3.7}$$

$$a_0 = (1 + gm_cRA)r_{oc} + RA + R_1 \quad \text{Equation 3.8}$$

$$a_1 = gm_5R_2gm_cR_1r_{oc}C_cRA + gm_5R_2R_1C_cRA + gm_cRAR_{oc}(R_1C_1 + R_2(CL + C_c)) + R_1RA(C_c + C_A) + RA(R_1C_1 + R_2CL) + R_1R_2(CL + C_c) + r_{oc}(R_2C_c + RA(C_c + C_A)) \quad \text{Equation 3.9}$$

$$a_2 = (gm_cRA + 1)R_2C_1R_1r_{oc}(CL + C_c) + R_2r_{oc}RAC_c(CL + C_A) + R_1R_2C_cRACA + R_2CLR_A(R_1(C_1 + C_c + C_A) + r_{oc}CA) + R_1C_1RA(r_{oc}(C_c + C_A) + R_2CL) \quad \text{Equation 3.10}$$

$$a_3 = R_1C_1R_2r_{oc}RA(CLCA + CLC_c + C_cCA) \quad \text{Equation 3.11}$$

In the above expression  $R_k$  and  $C_k$  are the impedance at respective nodes. Simplifying the above expression by making the assumption  $g_m R_k \gg 1$ , and  $C_L, C_c \gg C_1, C_A$ , the above can be expressed as

$$b_0 \approx g_m R_A r_{oc} \quad \text{Equation 3.12}$$

$$b_1 \approx R_A r_{oc} (C_c + C_A) \quad \text{Equation 3.13}$$

$$a_0 \approx (g_m R_A + 1) r_{oc} \quad \text{Equation 3.14}$$

$$a_1 \approx g_m R_2 R_1 r_{oc} C_c (g_m R_A + 1) \quad \text{Equation 3.15}$$

$$a_2 \approx (g_m R_A + 1) R_2 C_1 R_1 r_{oc} (C_L + C_c) + R_2 C_2 R_A [r_{oc} (C_c + C_A) + R_1 (C_c + C_A + C_1)] \quad \text{Equation 3.17}$$

$$a_3 \approx R_1 C_1 R_2 r_{oc} R_A (C_L C_A + C_L C_c + C_c C_A) \quad \text{Equation 3.18}$$

From the above simplified expressions the location of the zero from Equation 3.4 can be evaluated as shown below. Evidently, the zero is in the left half plane.

$$z_1 \approx -\frac{b_0}{b_1} = -\frac{g_m}{C_c + C_A} \quad \text{Equation 3.19}$$

Further, assuming the pole  $|p_1| \gg |p_2|, |p_3|$  the dominant real pole is given as

$$p_1 \approx -\frac{a_0}{a_1} = -\frac{1}{g_m R_2 R_1 C_c} \quad \text{Equation 3.20}$$

Now for  $s \gg p_1$ , the denominator of the transfer function  $D(s)$ , can be approximated as

$$D(s) \approx \left(1 - \frac{s}{p_1}\right) \left(1 + \frac{a_2}{a_1} s + \frac{a_3}{a_1} s^2\right) \quad \text{Equation 3.21}$$

From Equation 3.21 the non dominant poles can be derived. Assuming the two non dominant poles are real and spaced wide apart when  $\left(\frac{a_2}{a_1}\right)^2 \gg 4 \left(\frac{a_3}{a_1}\right)$ . The above condition is satisfied when

$$gm_c \gg \frac{4gm_5C_c \left( \frac{C_L C_c}{C_L + C_c} + C_A \right)}{C_1(C_L + C_c)} \approx \frac{4gm_5C_c (C_c + C_A)}{C_1 (C_L + C_c)} \quad \text{Equation 3. 22}$$

The above condition states that a large transconductance is required for common gate amplifier. However, when the above condition is met the non dominant poles relocate to the following locations

$$p_2 \approx -\frac{a_1}{a_2} = -\frac{gm_5C_c}{C_1(C_c + C_L)} \approx -\frac{gm_5C_c}{C_1C_L} \quad \text{Equation 3. 23}$$

$$p_3 \approx -\frac{a_2}{a_3} = -\frac{gm_c}{\left( \frac{C_c C_L}{C_L + C_c} \right)} + \frac{1}{(R_1 || r_{oc})C_1} \quad \text{Equation 3. 24}$$

The unity-gain frequency of the Op Amp is given as:

$$f_{uf} \approx \frac{\omega_{un}}{2\pi} = \frac{|p_1|A_V}{2\pi} = -\frac{gm_1}{2\pi C_c} \quad \text{Equation 3. 25}$$

From Equation 3.23 the non-dominant pole, when using indirect feedback compensation, is located at  $-\frac{gm_5C_c}{C_L C_1}$  while the second pole for Miller compensation was located at  $-\frac{gm_5}{C_1 + C_L}$ .

By comparing the two equations, we can examine that the second pole,  $p_2$ , has moved further away from the dominant pole by a factor of approximately  $C_c/C_1$ . Furthermore the LHP zero adds to the phase response near the unity gain frequency and thus improves the phase margin.

The overall transfer function of the system can be express as

$$\frac{V_{out}}{V_d} = \frac{\omega_{un}}{s} \cdot \frac{1}{1 + \frac{s}{\frac{gm_5C_c}{C_L C_1}}} \cdot \frac{1 + \frac{s}{\frac{gm_c}{C_c + C_A}}}{1 + \frac{s}{\frac{gm_c}{\left( \frac{C_L C_c}{C_L + C_c} \right)}}} \quad \text{Equation 3. 26}$$

Thus the condition on  $gm_c$  can be re-written as the following

$$f_{T6c} > \frac{gm_c}{C_c + C_A} > 4 \frac{gm_5 C_c (C_c + C_A)}{C_1 (C_L + C_C)} \quad \text{Equation 3. 27}$$

$$f_{T6c} > |z_1| > f_{T5} \cdot \frac{4C_c(C_c + C_A)}{(C_2 + C_C)} \quad \text{Equation 3. 28}$$

The above argument implies that now we can achieve pole splitting with a much lower value of compensation capacitor ( $C_c$ ) and a lower value of second stage transconductance ( $gm_5$ ). Conversely, lower value for  $gm_2$  translates into lower power as the bias current can be reduced. On the other hand, we can achieve higher unity gain frequency for the Op Amp without affecting stability and hence obtain a higher speed amplifier or drive a larger load capacitor for a given phase margin[21]. Analytically the reason the non-dominant pole shifted to a higher frequency is because the compensation capacitor now does not load the first stage output. Also Equation 3.22 is a key requirement for this architecture as it expresses the condition with respect to the transition frequency ( $f_T$ ) of transistor M6 and M5 the common gate amplifier and output stage respectively. It signifies that the indirect path has to be much faster than the output stage which thus relocates non dominant pole to higher frequency and thus improving the unity gain frequency. Blatantly observing, indirect feedback compensation can lead to the design of Op Amps with significantly lower power, higher speed and lower layout area.

Observing Equation 3.24, the location of the third non-dominant pole is further away from the second pole as long the  $gm_{cg}$  is large, and  $R_1$ ,  $C_1$  are small. Thus the third non dominant pole does not affect the phase margin.

Now considering if the condition in Equation 3.22 is not met then the poles are complex in nature and are defined below. The real part of the conjugate pole pair is given by

$$Re(p_{2,3}) = -\sqrt{\frac{a_1}{a_3}} = -\sqrt{\frac{gm_5 \cdot gm_c}{C_1 [C_L + (1 + \frac{C_L}{C_c}) C_A]}} \approx \sqrt{\frac{gm_5 \cdot gm_c}{C_1 C_L}} \quad \text{Equation 3. 28}$$

The damping factor for the complex poles is

$$\delta = \frac{a_2}{2\sqrt{a_1 a_3}} \approx \frac{1}{2C_c} \sqrt{\frac{C_1 C_L}{gm_5}} \quad \text{Equation 3. 29}$$

Also it can be observed that the

$$Re(p_{2,3}) \approx \frac{gm_5}{C_L} \sqrt{\frac{gm_c C_L}{C_1 gm_2}} \gg \frac{gm_5}{C_L} \quad \text{Equation 3. 30}$$

The non dominant pole is much further away from  $p_1$  as long as the transconductance of the common gate amplifier is large and the parasitic at node 1 is kept low.

### 3.3 Indirect Feedback using Cascoded Loads

Many operational amplifiers commonly have cascoded first stage or subsequent cascoded stages to obtain a high dc gain. When using a cascoded first stage, a low impedance internal node is easily available. This low impedance internal node can then be used to indirectly feedback the compensation current. Figure 3-4 depicts an implementation of an indirect feedback using cascoded current mirror load.

In this topology the common gate amplifier is embedded inside the cascoded current mirror load. Node A forms the low impedance needed for indirect feedback current to node  $V_1$ . The small signal mode for the following topology is the same as in Figure 3-3, where the common gate amplifier is the cascode transistor  $M_{c2}$ . Similar to the common gate amplifier analyzed in the previous section, the LHP zero and the three poles are given by Equations 3.19-3.24, where  $gm_{cg}$  is the transconductance of the cascode transistor  $gm_{c2}$ . The cascoded loads topology saves area and power as an additional common gate stage is not required. However, the reduction in power comes at the cost of flexibility choosing the transconductance of  $gm_{cg}$ , which controls the location of the LHP zero.

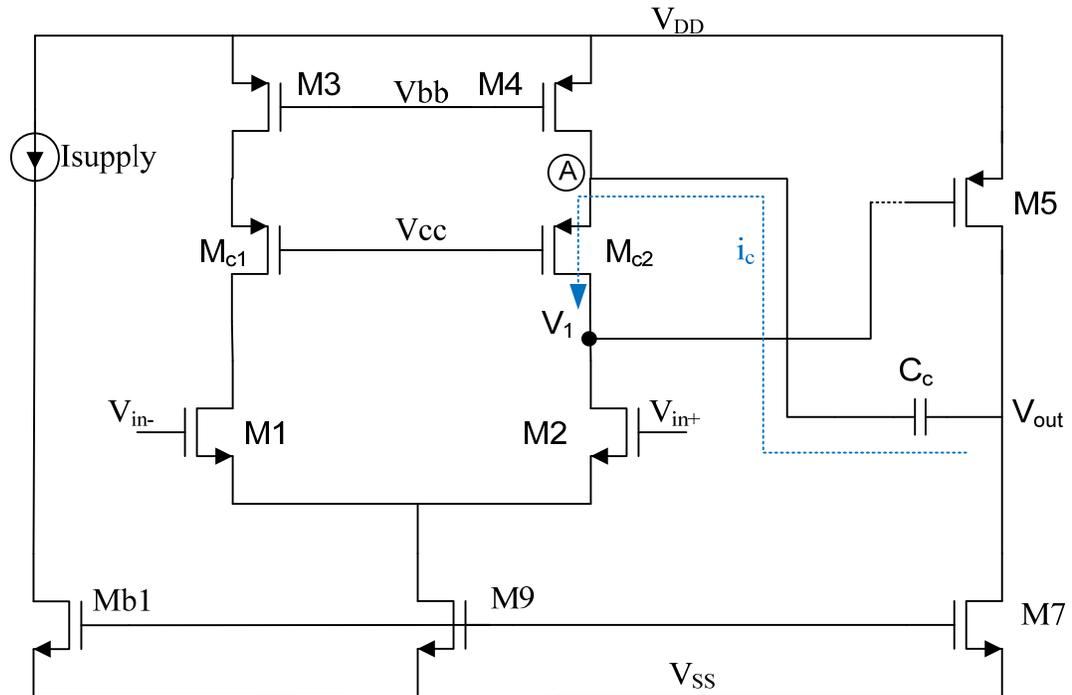
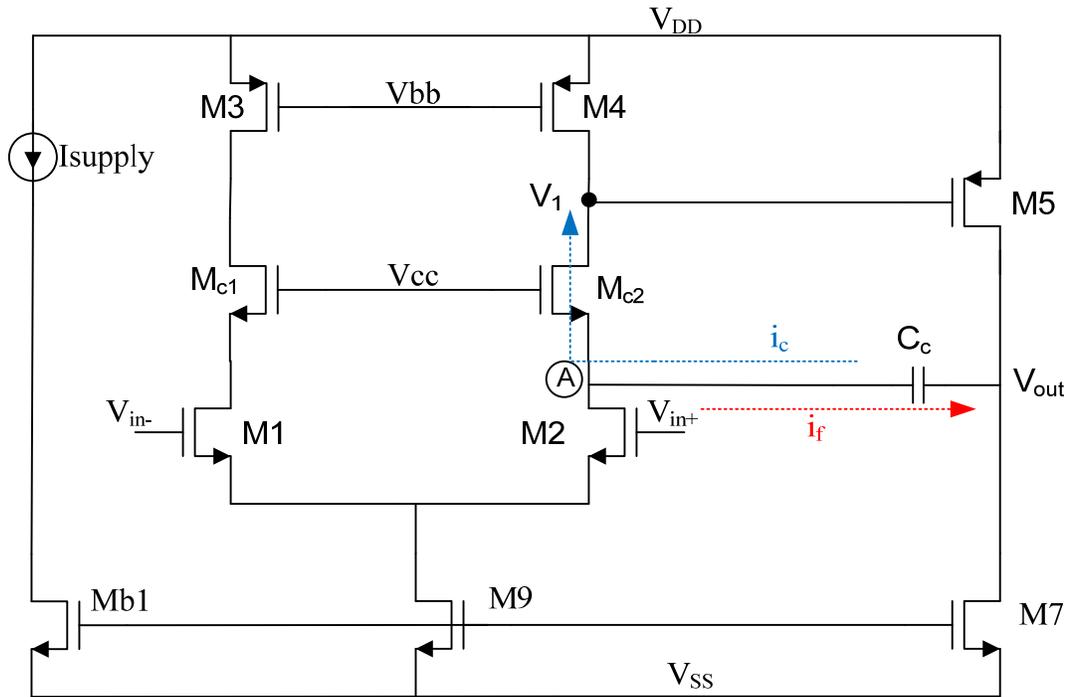


Figure 3-4 A two stage Op Amp with cascoded loads. The compensation capacitor is connected to node A for indirect feedback.

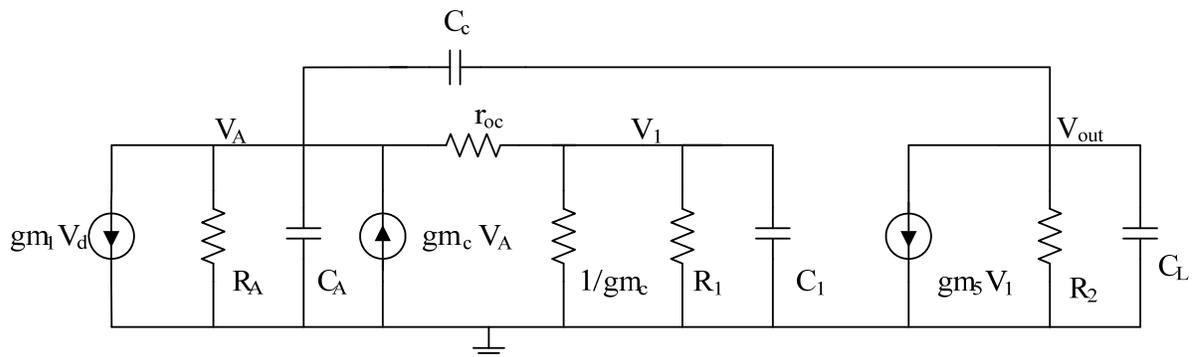
### 3.4 Indirect Feedback using Cascoded Differential Pair

Other than a cascoded current mirror load, a cascoded differential pair could also be used to feedback the compensation current indirectly. Figure 3-5 shows the schematic for implementing such architecture. The compensation capacitor is connected to the low impedance node A. However, this topology is not the same as the cascode current mirror load, as the common gate amplifier is not isolated from the input. This leads to both an indirect feedback current, as well as a feedforward current through the compensation capacitor to the output. The feedforward current can only be eliminated if all the current at the source of  $M_{c2}$  is passed through the drain and not through the compensation capacitor, which is only possible when the transconductance of  $M_{c2}$  is infinite.



**Figure 3-5** A two stage Op Amp with cascoded differential pair. The compensation capacitor is connected to node A for indirect feedback.

The small signal model for the two stage amplifier with cascoded differential pair is shown below in Figure 3-6. A small signal is required to understand the implications of the feedforward current through the compensation capacitor.



**Figure 3-6** Small signal model for Op Amp with cascoded differential pair. The compensation capacitor is connected to node A.

On doing the nodal analysis as in previous section, the Kirchhoff equations can be written as:

$$-gm_1V_d + \frac{V_A}{R_A} + V_A sC_A + gm_cV_a + \frac{(V_A - V_1)}{r_{oc}} + sC_c(V_A - V_{out}) = 0 \quad \text{Equation 3.31}$$

$$-gm_cV_A + \frac{V_1}{R_1} + V_1 sC_1 + \frac{(V_1 - V_A)}{r_{oc}} = 0 \quad \text{Equation 3.32}$$

$$gm_5V_1 + \frac{V_{out}}{R_2} + V_{out} sC_2 + sC_c(V_{out} - V_A) = 0 \quad \text{Equation 3.33}$$

Solving the above simultaneous equations, the below small signal transfer function is obtained.

$$\frac{V_{out}}{V_s} = -A_v \left( \frac{b_0 + b_1s}{a_0 + a_1s + a_2s^2 + a_3s^3} \right) \quad \text{Equation 3.34}$$

The coefficients are given as:

$$A_v = gm_1R_1gm_5R_2 \quad \text{Equation 3.35}$$

$$b_0 = (1 + gm_c r_{oc})R_A \quad \text{Equation 3.36}$$

$$b_1 = -(R_A C_c (r_{oc} + R_1)) / (gm_2 R_1) \quad \text{Equation 3.37}$$

$$b_2 = -(R_A r_{oc} C_c C_1) / gm_5 \quad \text{Equation 3.38}$$

$$a_0 = (1 + gm_c R_A) r_{oc} + R_A + R_1 \quad \text{Equation 3.39}$$

$$a_1 = gm_5 R_2 gm_c R_1 r_{oc} C_c R_A gm_5 R_2 R_1 C_c R_A + gm_c R_A r_{oc} (R_1 C_1 + R_2 (C_L + C_c)) R_1 R_A (C_c + C_A) + R_A (R_1 C_1 + R_2 C_L) R_1 R_2 (C_L + C_c) + r_{oc} (R_2 C_c + R_A (C_c + C_A) + R_1 C_1 + R_2 C_L) \quad \text{Equation 3.40}$$

$$a_2 = (gm_c R_A + 1) R_2 C_1 R_1 r_{oc} (C_L + C_c) R_2 r_{oc} R_A C_c (C_L + C_A) + R_1 R_2 C_c R_A C_A + R_2 C_L R_A (R_1 (C_1 + C_c + C_A) + r_{oc} C_A) + R_1 C_1 R_A (r_{oc} (C_c + C_A) + R_2 C_L)$$

$$a_3 = R_1 C_1 R_2 r_{oc} R_A (C_L C_A + C_L C_c + C_c C_A) \quad \text{Equation 3.41}$$

The above expressions can be simplified by making the approximations that  $gm_k R_k \gg 1$ , and  $C_L, C_c \gg C_1, C_A$ . The simplified has the same denominator as Equation 3.21. However, the numeration coefficients and the locations of the two zeros are expressed below:

$$z_{1,2} = -\frac{1}{2(R_1 || r_{oc})C_1} \pm \sqrt{\frac{1}{4(R_1 || r_{oc})^2 C_1^2} + \frac{gm_5 gm_c}{C_c C_1}} \quad \text{Equation 3.42}$$

From Equation 3.42 it can be noticed that the zeros are real and one of the zero is in the LHP while the other in RHP.

$$z_{LHP} = -\frac{1}{2(R_1 || r_{oc})C_1} - \sqrt{\frac{1}{4(R_1 || r_{oc})^2 C_1^2} + \frac{gm_5 gm_c}{C_c C_1}} \quad \text{Equation 3.43}$$

$$z_{RHP} = -\frac{1}{2(R_1 || r_{oc})C_1} + \sqrt{\frac{1}{4(R_1 || r_{oc})^2 C_1^2} + \frac{gm_5 gm_c}{C_c C_1}} \quad \text{Equation 3.44}$$

If assuming the condition  $\sqrt{\frac{gm_5 gm_c}{C_c C_1}} \gg \frac{1}{4(R_1 || r_{oc})^2 C_1^2}$ , the locations of the zeros can be simplified as

$$z_{LHP} \approx -\sqrt{\frac{gm_5 gm_c}{C_c C_1}} \quad \text{Equation 3.45}$$

$$z_{RHP} \approx \sqrt{\frac{gm_5 gm_c}{C_c C_1}} \quad \text{Equation 3.46}$$

The approximate pole locations for this topology are exactly the same as derived for cascoded load indirect compensation. Furthermore, the location of the right half plane is so far away from the unity gain frequency, that it is unlikely it would degrade the Op Amps frequency response. Considering the poles of the system are complex, then from Equation 3.28 it can be seen the poles are at the same frequency as the zero. Thus the complex poles and zero are clustered, and can be approximated by two real left half plane poles and one right half plane zero.

### 3.4 Other Operational Amplifier Specifications

Apart from the speed of the amplifier, there are other specifications that need to be addressed. This section provides an overview and common techniques used in literature to improve and enhance those specifications.

### 3.4.1 Slew Rate Limitations in Op Amps

Op Amps used in feedback circuits exhibit a large-signal behavior called “slewing”. Slew rate represents the maximum rate at which a capacitive load is charged and discharged. The slew rate is thus defined as

$$SR = \frac{dV_{out}}{dt} = \frac{I_s}{C_L} \quad \text{Equation 3.47}$$

The Op Amp architectures presented in previous sections, Figure 3-2, 3-4, 3-5, are all Class A type amplifiers. In Class A Op Amps the charging and discharging of the load capacitor is provided by the fixed current source. This fundamentally limits the slew rate of the amplifier. Figure 3-7 shows the slew rate limitations in these amplifiers. During charging of the capacitor  $C_L$ , there is no slew rate limitation, as the transistor gate M5 is completely pulled, and the transistor sources current following the square law model. However while discharging the capacitor, the fixed current source  $I_{SS2}$  limits the rate. The discharging slew rate is thus given by  $SR = \frac{I_{SS2}}{C_L}$ , where  $I_{SS2}$  is the output bias current [22]. Indirectly this implies that in class A type Op Amps, higher current need to be burned for achieving high slew rate. Furthermore, driving large loads of 100pf and above requires an extremely large quiescent current. To solve the problem of high power requirement for slew rate, Class AB type output stages can be designed. This is explained in Figure 3-8.

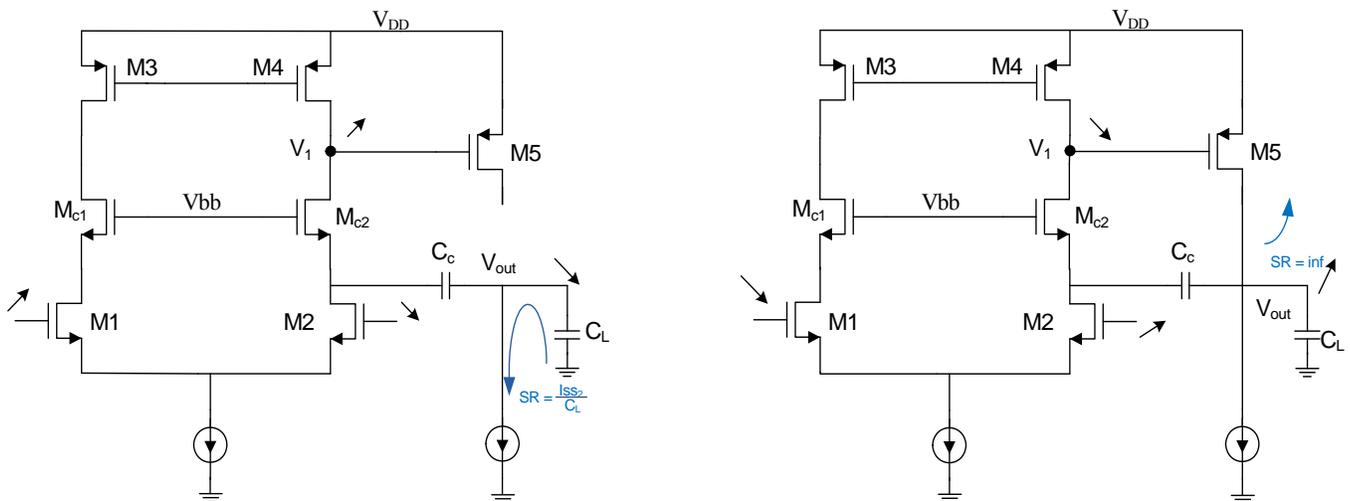
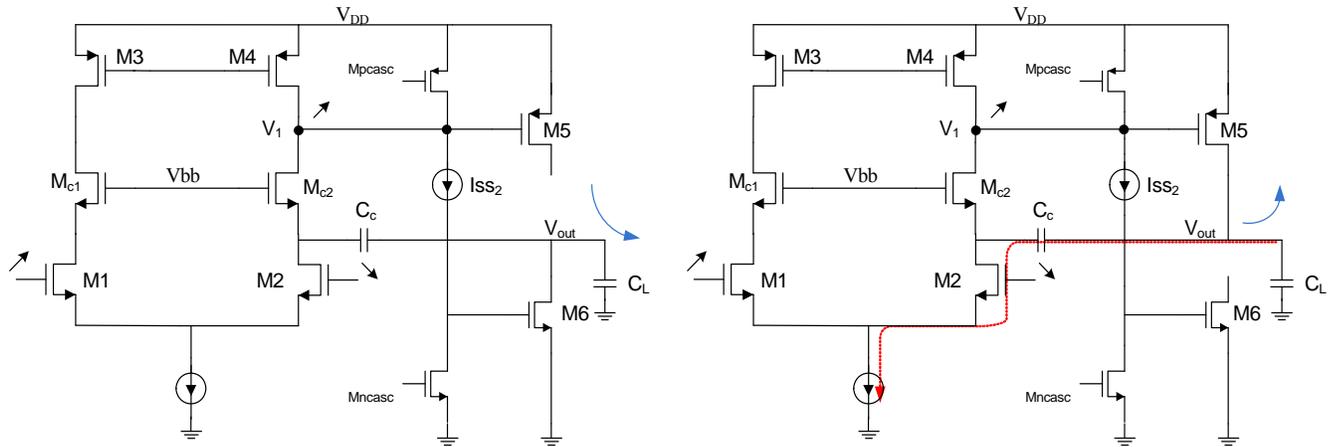


Figure 3-7 Slew Rate limitation in Class A type amplifiers. In this case, during discharging the output is limited by the current source  $I_{SS2}$ . While charging there is ideally no limitation.

The Class AB output stage is realized by having a floating current source biased between the output stages transistors behaving like a push pull [3]. The floating current source acts like a battery turning M5 on hard and turning off M6 when charging, and turning M6 on and turning off M5 during discharging.



**Figure 3-8 Class AB output stage improving the slew rate of the Op Amp during discharging phase. However the charging is still limited by the compensation capacitor being charged by Iss1 current source.**

as a new slew rate limitation appears during charging as shown in Figure 3-8. The capacitor  $C_c$  needs to be charged, and the first stage current source provides the current to charge it. Thus during charging the slew rate is given by  $SR = \frac{I_{SS5}}{C_c}$ . However this slew rate is much higher than the Class A type, as  $C_c$  is much smaller than the load capacitor  $C_L$ . Furthermore, indirect compensation achieves higher slew rate in comparison to miller compensation as the  $C_c$  value is much smaller.

### 3.4.2 Random Offset

Offset is an important dc specification for an operational amplifier as it limits the dc precision of the amplifier. Suppose the differential pair of Figure 3-2 is to amplify a small input voltage. Then in a cascade of direct-couple amplifiers the dc offset may experience so much gain that it drives the later stage into the nonlinear operation. More importantly the effect of offset limits the performance of an amplifier if it is used to determine whether an

input signal is greater or less than a reference. In such a case the input-referred offset voltage imposes a lower bound on the minimum  $V_{in}-V_{REF}$ .

Offset for operational amplifier architecture shown in Figure 3-2 has been previously derived in [5]. The expression below is the random input-referred offset voltage

$$V_{OS,N} = \frac{(V_{gs} - V_{th})_N}{2} \left[ \frac{\Delta(W/L)}{(W/L)} \right]_N + \Delta V_{th,N} \quad \text{Equation 3. 48}$$

$$V_{OS,P} = \frac{(V_{sg} - V_{th})_P}{2} \left[ \frac{\Delta(W/L)}{(W/L)} \right]_P + \Delta V_{th,P} \quad \text{Equation 3. 49}$$

$$V_{OS} = V_{OS,P} + V_{OS,N} \quad \text{Equation 3. 50}$$

Observing Equation 3.48 and 3.49 it can be noticed increasing the input pair area and current load area reduces the random input-referred offset voltage. Other techniques such as resistive degeneration can be used to reduce the contribution of the current load offset ( $V_{OS,P}$ ). Offset cancellation techniques as in [23] can also be implemented to cancel and reduce the input referred offset specification.

### 3.4.3 Common Mode and Power Supply Rejection Ratio

An important aspect of the differential amplifier is its ability to reject a common signal applied to both inputs. Often, in analog systems, signals are transmitted differentially, and the ability of an amplifier to reject coupled noise into each line is very desirable. Thus common mode rejection ratio (CMRR) is an important specification for an Op Amp. The expression of common mode gain has been derived in [3, 8]

$$A_C = \frac{V_{out}}{V_{CM}} = -\frac{1}{2R_o} \frac{1}{gm_{3,4}} = -\frac{1}{2gm_{3,4}} \quad \text{Equation 3. 51}$$

$$CMRR = 20 \log \left( \frac{A_D}{A_C} \right) = 20 \log [gm_{1,2}(r_2 || r_4) \cdot 2gm_{3,4}R_o] \quad \text{Equation 3. 52}$$

The larger the CMRR better the performance of the amplifier. Many techniques such as high impedance current sources and regulated circuits have been proposed in literature to improve the common mode performance of the Op Amp.

Power supply rejection ratio (PSRR) is a parameter of high importance in MOS amplifier design [3, 8]. With high integration of analog and digital systems, separate analog and digital supply buses are often run on chip. However it is still hard to avoid some coupling of digital noise into the analog supplies. Furthermore, many systems employ switching regulators which introduce power supply noise into supply voltage lines. The expression for PSRR is given in [5] as

$$PSRR \approx gm_N(r_1 || r_4) \quad \text{Equation 3.53}$$

The basic circuit of Figure 3-2 exhibits very poor high frequency rejection from the positive supply rail. The main reason is that as the applied frequency increases, the impedance of the compensation capacitor decreases, effectively shoring the drain of M5 to its gate for ac signals. The gain from the positive supply to the output approaches unity and stays there out to very high frequencies. Several alternative amplifier architectures have evolved which alleviate this problem; one such is the proposed indirect feedback frequency compensation using a common gate cascode. The resulting positive PSRR at high frequencies is greatly improved. Others include sub regulated power supply rails which also provide extremely good PSRR performance.

### 3.5 Pre-Design Procedure Guidelines

This methodology is intended for low-power analog and digital signals where the weak as well as moderated inversion regions are often used because they provide good compromise between speed and power consumption. The  $g_m/I_d$  ratio is indeed a universal characteristic of all transistors formed by the same process.

MOS transistors are either in strong inversion or in weak inversion. Mainstream methods assume generally strong inversion and use the transistor gate voltage overdrive ( $V_{OV}$ ) as the key parameter, where  $V_{OV} = V_{GS} - V_t$ . If we consider a simple common source amplifier, the power and bandwidth are given by the following equations

$$P = \frac{1}{2} \frac{V_{DD}}{R_L} A_{DC} V_{OV} \quad \text{Equation 3.54}$$

$$\omega_{-3dB} = \frac{3}{2} \frac{R_L}{R_i} \frac{\mu}{L^2} V_{OV} \quad \text{Equation 3.55}$$

With the assumed fixed design specifications, and a given technology ( $\mu$ ,  $L_{min}$ ), both power and bandwidth of our circuit are completely determined by the value of  $V_{OV}$ . Making  $V_{OV}$  small to save power also means that we lose bandwidth. This makes intuitive sense since

$$\frac{W}{L} = \frac{gm}{\mu C_{ox} V_{OV}} \quad \text{Equation 3.56}$$

With  $g_m$  and  $L$  fixed, smaller  $V_{OV}$  translates into bigger (wider) device, and thus large  $C_{gs}$ . So it can be concluded that  $V_{OV}$  is not a good design parameter. What we really want from MOS transistor is

- Large  $g_m$  without investing much current
- Large  $g_m$  without large  $C_{gs}$

To quantify how good of a job our transistor does, we can therefore define the following “figure of merits (FOM)”.

- Transconductor Efficiency:

$$T_e = \frac{gm}{I_D} \quad \text{Equation 3.57}$$

- Transit Frequency:

$$\omega_T = \frac{gm}{C_{gs}} \quad \text{Equation 3.58}$$

Figure 3-9 shows the Transconductor Efficiency ( $gm/I_D$ ) versus the  $V_{ov}$  (over drive voltage) of the transistor with fixed  $W/L$  ratio and varying lengths. From the graph it can be inferred for AMI 0.5 $\mu\text{m}$  CN process to achieve optimal transconductor efficiency the over drive voltage from the transistor should be between 0.1-0.2V. After 0.4V the increase in  $gm$  with increase current is not efficient. Thus if the  $V_{OV}$  of the transistor is high, then increasing the current would only increase the  $gm$  of the transistor marginally. Similarly increasing the size would give a marginal increase in transistor transconductance. Figure 3-9 also shows the  $f_T$  vs  $V_{ov}$ , and for obtaining the highest  $f_T$  minimum transistor length (0.6 $\mu\text{m}$ ) should be used in the design. A trade-off is seen between the transconductance efficiency and transit frequency ( $f_T$ ). Increasing the overdrive voltage higher speed transistor, however the transconductance efficiency is poor. The figure of merits should always be kept in mind during designing an amplifier for a particular process.

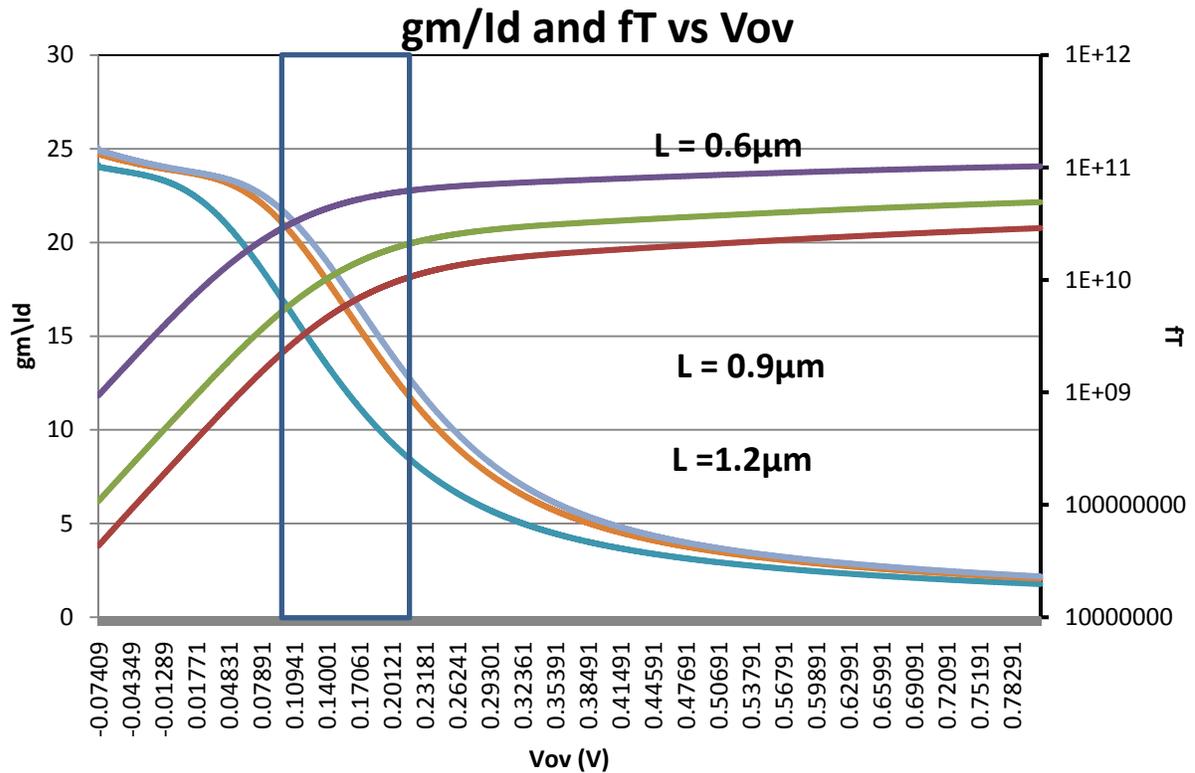


Figure 3-9  $gm/I_D$  and  $f_T$  versus  $V_{ov}$  ( $V_0$ )

### 3.7 Indirect Feedback Design Procedure

This section provides a guideline for designing amplifiers with indirect feedback compensation method. The schematic for this particular design procedure is shown in Figure 3-9. The architecture is a two stage single ended Op Amp with a Class A output stage. A common mode feedback is provided to bias the first stage PMOS current load.

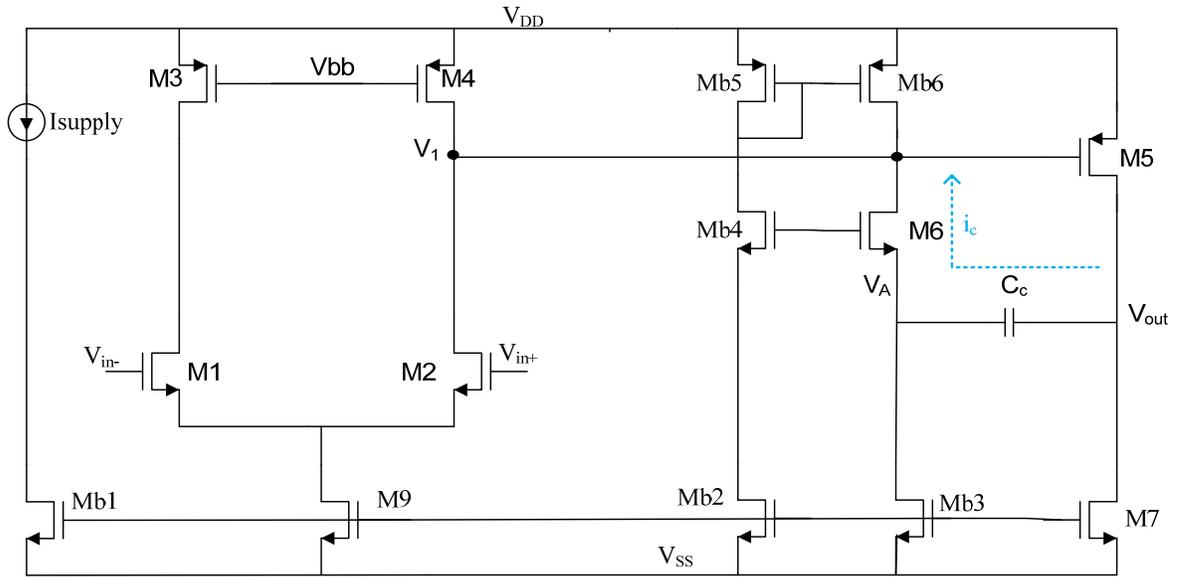


Figure 3-10 Two stage amplifier with Class A output stage and Indirect Feedback Compensation

#### 3.7.1 Input Referred Thermal Noise Spectral Density

The procedure starts with the thermal noise requirement for the Op Amp. Neglecting the flicker noise requirement, which contributes to the low frequency noise spectrum, the input referred noise voltage can be expressed as shown in Equation 3.59.

$$S_n(f) = 2 \cdot 4kT \frac{2}{3} \frac{1}{gm_{1,2}} \left[ 1 + \frac{gm_{3,4}}{gm_{1,2}} \right] \quad \text{Equation 3.59}$$

To minimize noise, we assume  $gm_{3,4} < gm_{1,2}$  (which can be easily met) and calculate the transconductance gain of transistors  $M_{1,2}$  from Equation 3.60

$$gm_{1,2} = \frac{16}{3} \frac{kT}{S_n(f)} \quad \text{Equation 3.60}$$



### 3.7.3 Output Swing

By defining  $V_{HR}^{out}$  as the Op Amp headroom voltage at output i.e.,

$$V_{HR}^{out+} = V_{DD} - V_{out(max)} \quad \text{and} \quad V_{HR}^{out-} = V_{out(min)} - V_{SS} \quad \text{Equation 3.64}$$

According to Figure 3-11 it is easy to show that

$$V_{HR}^{out+} \leq V_{eff5} \quad \text{and} \quad V_{HR}^{out-} \leq V_{eff11} \quad \text{Equation 3.65}$$

### 3.7.4 Common-Mode Range

Defining  $V_{HR}^{CM}$  as the Op Amp head room voltage of the input common-mode range,

i.e.,

$$V_{HR}^{CM+} \leq V_{DD} - V_{CM(max)} \quad \text{and} \quad V_{HR}^{CM-} \leq V_{CMt(min)} - V_{SS} \quad \text{Equation 3.66}$$

According to Figure 3-11 it is easy to show that

$$V_{HR}^{CM+} = V_{eff3} - V_{tn} \quad \text{and} \quad V_{HR}^{CM-} = V_{eff9} + V_{tn} + V_{eff1,2} \quad \text{Equation 3.67}$$

### 3.7.3 Indirect Frequency Compensation and Miller Capacitor

Recalling the expression from 3.19 -3.25 helps in analyzing the frequency response of an amplifier with indirect feedback frequency compensation. These expressions are recollected below form easier analysis.

$$\text{Dominant Pole: } p_1 \approx -\frac{a_0}{a_1} = -\frac{1}{g_{m5}R_2R_1C_c}$$

Further if the condition  $g_{m6} \gg \frac{4g_{m5}C_c(C_c+C_A)}{C_1(C_L+C_C)}$  is met, then two non-dominant real poles and one left half plane zero is obtained from the transfer function, given below:

$$z_1 \approx -\frac{b_0}{b_1} = -\frac{g_{mc}}{C_c + C_A}$$

$$p_2 \approx -\frac{a_1}{a_2} = -\frac{g_{m5}C_c}{C_1(C_c + C_L)} \approx -\frac{g_{m5}C_c}{C_1C_L} \quad \text{and} \quad p_3 \approx -\frac{a_2}{a_3} = -\frac{g_{mc}}{\left(\frac{C_cC_L}{C_L + C_c}\right)} + \frac{1}{(R_1 || r_{oc})C_1}$$

Finally the unity gain frequency is obtained by

$$f_{uf} \approx \frac{\omega_{un}}{2\pi} = \frac{|p_1|A_V}{2\pi} = -\frac{g_{m1}}{2\pi C_C}$$

The compensation capacitor then can be calculated to be:

$$C_c = \frac{g_{m1}}{2\pi f_{uf}} \quad \text{Equation 3. 68}$$

Moving forward, making the following assumptions:

$$\frac{|z|}{|p_2|} \approx \frac{g_{mc}}{g_{m5}} \cdot \frac{C_1C_L}{C_c^2} > 1 \quad \text{Equation 3. 69}$$

$$\frac{|p_3|}{|z|} \approx \frac{C_L + C_c}{(C_L C_c)(C_A + C_c)} \cong \frac{1}{C_c^2} \gg 1 \quad \text{Equation 3. 70}$$

Assumption in Equation 3.57 is valid because to have real poles for the system (Equation 3.22)  $g_{mc} > g_{m2}$  by a factor of  $4C_c/C_1$  which is much greater than one, and the geometric mean of  $C_1C_L$  is larger than  $C_c^2$ . Nevertheless, it should be verified these ratios are greater than one during the design, as the system is modeled on the above assumptions.

The equations 3.69-3.70 ensure that the system behaves as single dominant, and single non-dominant pole, and  $GBW \approx UGF$ . Thus  $V_{out}/V_{in}$  can be reduced to

$$\frac{V_{out}}{V_s} = \frac{\omega_{uf}}{s} \times \frac{1}{1 - \frac{s}{p_2}} \quad \text{Equation 3. 71}$$

Following Pennisi [24] constraints and design strategies for sizing common gate amplifier M5 can be developed. The phase margin with 100% feedback can be shown to be

$$\varphi_M = \tan^{-1} \frac{|p_2|}{\omega_{uf}} = \tan^{-1} \frac{\omega_{T5}C_c}{\omega_{uf}C_L} \quad \text{Equation 3. 72}$$

$$gm_5 = \tan(\varphi_M)\omega_{uf}C_L \frac{C_1}{C_C} \quad \text{Equation 3.73}$$

The above equation 3.73 helps in sizing the transistor M5. Equation 3.71 also provides insight regarding the higher power saving achieved from the indirect feedback compensation. The factor  $C_1/C_C$  is less than one significantly and thus  $gm_5$  is reduced, indirectly less power required. Another degree of freedom, the current in M5, is available if a class AB output stage is implemented. There is flexibility in achieving the  $gm_5$  requirement by spending area or current. The transistor size of M5 can be decided by solving the following equations:

$$\omega_{T5} = \frac{gm_5}{C_{gs5}} = \frac{3}{2} \frac{\mu_p}{L_5^2} V_{eff5} \quad \text{Equation 3.74}$$

$$V_{eff5} = \frac{L_5^2 2\omega_{uf}C_L \tan \varphi_M}{3\mu_p C_C} \quad \text{Equation 3.75}$$

To obtain a high speed output stage  $L_5 = L_{min}$ , as seen from Figure 3-9. Simultaneously it should be verified if output swing requirements from Equation from 3.65 are met. Also it should be made sure that the transistor is not in sub-threshold operation and thus  $V_{eff5}$  should be greater than 50mV.

Output stage current can be decided by performing tradeoff between area and power tradeoff for the common gate stage and output stage. Reconsidering the Equation 3.22 it can be approximated how much larger  $gm_5$  is in comparison to  $gm_6$ .

$$gm_6 > \frac{4gm_5 C_c (C_c + C_A)}{C_1 (C_L + C_C)} \approx 4gm_5 \frac{C_c^2}{C_1 C_L} \quad \text{Equation 3.76}$$

The geometric mean of  $C_1 C_L$  is less than one and the total factor is about 0.5~2.

Thus to the first order approximation  $gm_6 \approx (2-8)gm_5$ . Thus the current between the common

gate stage and the output stage can be split to a ratio 2~4. The output stage current and  $M_5$  width can be calculated as following:

$$I_5 = \frac{(I_{Total} - I_1)}{(2 \sim 4)} \quad \text{Equation 3.77}$$

$$W_5 \gg \frac{2I_5L_5}{\mu_p C_{ox} V_{eff5}} \quad \text{Equation 3.78}$$

Finally the transistor size and current requirement in the common gate can be determined using Equation 3.22 for achieving real poles.

$$gm_6 > \frac{4gm_5 C_c (C_c + C_A)}{C_1 (C_L + C_C)} \quad \text{Equation 3.79}$$

$$I_6 = I_{Total} - I_1 - I_5 \quad \text{Equation 3.80}$$

$$\left(\frac{W}{L}\right)_6 > \frac{gm_6^2}{4K_p I_{D6}} \quad \text{Equation 3.81}$$

### 3.7.6 Final Design Procedure

A design step for two-stage Op Amp (Figure 3-11) can be constructed as follows:

Step 1. From (3.60) we have

$$gm_{1,2} = \frac{16}{3} \frac{kT}{S_n(f)}$$

Step 2. From (3.68) we can calculate compensation capacitor

$$C_c = \frac{g_{m1}}{2\pi f_{uf}}$$

It should be noted that the compensation capacitor needs to be optimized again after the design procedure is complete. During simulation tweaking the compensation capacitor is required to obtain the appropriate stability.

Step 3. Using (3.62) the  $I_{D1,2}$  can be calculated

$$I_{D1,2} = \frac{SR_{INT}C_c}{2}$$

Step 4. From (3.62) and (3.63) the transistor size for  $M_{1,2}$  can be calculated

$$\left(\frac{W}{L}\right)_{1,2} = \frac{gm_{1,2}^2}{4K_n I_{D1,2}}$$

Step 5. From the output swing requirement (3.65),  $V_{eff5}$  and  $V_{eff11}$  must satisfy

$$V_{HR}^{out+} \leq V_{eff5} \quad \text{and} \quad V_{HR}^{out-} \leq V_{eff11}$$

Step 6. Following (3.75) the output transistor  $V_{eff5}$  can be determined

$$V_{eff5} = \frac{2L_5^2 \omega_{uf} C_L \tan \varphi_M}{3\mu_p C_c}$$

The above  $V_{eff5}$  has to meet the condition in step 5. Larger  $L_5$  can be tried, a max of  $2L_{min}$ . Increase  $L_5$  provides better performance over process variation.

Step 7. Calculate  $I_{D5}$  using the following

$$I_5 = \frac{(I_{Total} - I_1)}{2 \sim 4}$$

Step 8. Calculate  $V_{eff5}$  from (3.75) and use (3.77) to calculate  $W_5$

$$W_5 = \frac{2I_{D5}}{2K_p (V_{HR}^{out+})^2} L_5$$

Step 9. Using (3.79) calculate the transconductance of common gate

$$gm_6 > 4gm_5 \frac{C_c^2}{C_1 C_L}$$

Step 10. Using (3.80) calculate the current in the common gate amplifier

$$I_6 = I_{Total} - I_1 - I_5$$

Step 11. From step 8 and (3.81) the common gate transistor  $M_6$  can be calculated

$$\left(\frac{W}{L}\right)_6 > \frac{gm_6^2}{4K_p I_{D6}}$$

### 3.7 Figure of Merit

To perform a comparison in terms of speed among the many compensation approaches independently of the particular amplifier topology, design choices, and technology, a figure of merit (FOM) that relates the load capacitance  $C_L$ , the gain-bandwidth product  $\omega_{GBW}$ , and the total current consumption of the amplifier  $I_{Total}$  has been proposed [14]. This relation is shown in Equation 3.82. Similarly a comparison for the time domain slew rate can be expressed as in Equation 3.83. Finally, a comparison is required to measure the efficiency of the amplifier in comparison to a single stage, which is expressed in Equation 3.76.

$$IFOM_S = \frac{GBW * C_L}{I_{Total}} \quad \text{Equation 3. 82}$$

$$IFOM_L = \frac{SR * C_L}{I_{Total}} \quad \text{Equation 3. 83}$$

$$FOM_{SS} = \frac{\omega_{GBW}}{gm_T / C_L} \quad \text{Equation 3. 84}$$

$FOM_{SS}$  represents the ratio between the gain bandwidth of the amplifier in comparison to the gain bandwidth achieved from a pure single stage (such as a common source) with the same load and having a transconductance equal to  $gm_T$  (i.e., sum of each transconductance stages). Moreover, the transconductance is a key design parameter related to the power consumption and the amplifier silicon area.

## CHAPTER 4.

### 4.1 Introduction

This chapter discusses the design of a low power, high speed, general purpose Op Amp driving large capacitive loads, following the design procedure outline in section 3.6. The proposed Op Amp structure applies indirect feedback frequency compensation to achieve the high speed. The Op Amp employs the traditional two gain stages followed by a class A/B output stage. This approach overcomes some of the limitations of the single miller compensation which provides very low speed amplifier driving large capacitive load. With two gain stages, indirect feedback frequency compensation capacitor as small as 5 pF can be used to drive a 150 pF. As discussed in the former chapter, low power Op Amp can be designed by carefully choosing the appropriate current density and overdrive voltage to obtain maximum gm to power efficiency.

### 4.2 Design Example

A simple two stage Op Amp as shown in Figure 4.1 was designed for the purpose of demonstrating the indirect feedback frequency compensation. The Op Amp has a fully differential first stage, and thus need a common mode feedback circuit (CMFB). The output stage is a class A/B stage to achieve a high slew rate when charging a large capacitive load of 150 pF. A standard supply independent current source is also implemented to generate the reference current. The detail of each block will be explored in the following sections.

The required Op Amp specifications are mentioned in Table 4.1. The Op Amp is designed in AMI 0.5 C5N process. The process parameters are provided in Table 4.2. The design procedure illustrated in section 3.6 is used to design the Op Amp. Further optimization is performed to achieve higher performance specifications.

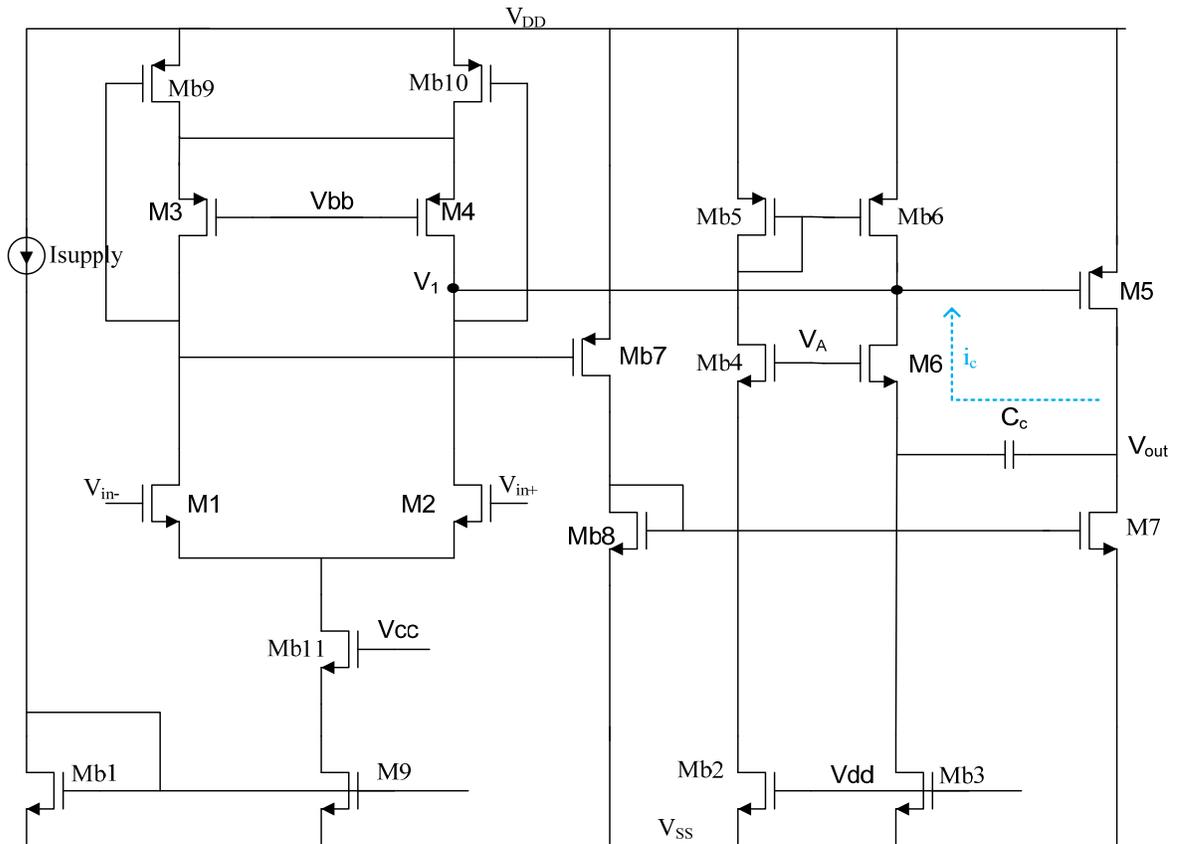


Figure 4-1 Two Stage Amplifier with Class A/B output stage and indirect feedback frequency compensation

Table 4-1 Two Stage Design Op Amp Specification

Op Amp Specification	
Supply Voltages	$\pm 1.25$ V
Load Capacitance: $C_L$	100 pF
Total Current	30 $\mu$ A
DC gain: $A_o$	70 dB
Unity-gain Frequency: $f_u$	2 MHz
Phase Margin: $\phi_M$	60°
Slew Rate: $SR$	1 V/ $\mu$ s
Input Common Mode Range: $V_{CMR}$	$\pm 1$ V
Output Swing: $V_{out \{max,min\}}$	$\pm 0.5$ V
Input Referred Noise	15 nV/ $\sqrt{\text{Hz}}$

**Table 4-2 AMI 0.5 C5N Process Parameters**

Process Parameters (AMI 0.5 Micron C5N)		
Parameters	NMOS	PMOS
$\mu \left[ \text{cm}^2/\text{Vsec} \right]$	458	212
$V_t$ [V]	0.7	-0.9
$T_{\text{ox}}$ [nm]	6.95	6.95

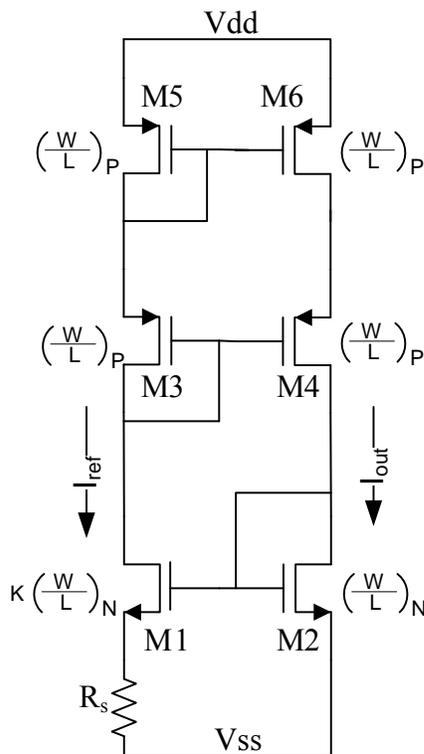
**Table 4-3: Transistor Sizing for Indirect Feedback Op Amp**

Op Amp Sizing		
Transistor	Multiplier	Size ( $\mu\text{m}$ )
$M_{1,2}$	2	4.05/0.9
$M_{3,4}$	2	3.6/2.4
$M_5$	6	10.05/1.5
$M_6$	12	15/1.05
$M_7$	6	1.65/1.05
$M_{9,b11}$	10	1.65/4.05
$M_{b1}$	1	1.65/4.05
$M_{b2}$	1	1.65/1.05
$M_{b3}$	12	1.65/1.05
$M_{b4}$	1	2.4/1.05
$M_{b5}$	1	12/1.05
$M_{b6}$	12	12/1.05
$M_{b7}$	2	3/1.2
$M_{b8}$	1	1.65/1.05
$M_{b9,10}$	10	1.95/0.6
$C_c$	-	5 pF
$I_{\text{supply}}$	-	1.25uA

Complete schematic of the amplifier along with the bias generator is attached in Appendix A. It is important to have some insight while designing the bias transistors in Figure 4-1. The next two section provide some insight in designing the bias generator and the sizing the bias transistors.

### 4.2.1 Bias Generator

Figure 4-2 depicts a supply independent bias generator used in this Op Amp design. The key idea behind supply independent biasing is that if  $I_{out}$  is to be completely independent of  $V_{dd}$ , then  $I_{ref}$  can be a replica of  $I_{out}$ . In Figure 4-2 it can be observed that each diode connected device feeds from a current source, and thus



**4-2 Supply Independent Bias Generator**

connected device feeds from a current source, and thus  $I_{out}$  and  $I_{ref}$  are relatively independent of  $V_{DD}$ . The derivation of the architecture in Figure 4-2 is completed in [razavi]. The  $I_{out}$  from the bias generator is then expressed in Equation 4.1

$$I_{out} = \frac{2}{\mu_n C_{ox} \left(\frac{W}{L}\right)_N} \cdot \frac{1}{R_s^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad \text{Equation 4.1}$$

It can be observed from the above expression, the current is independent of the supply voltage; however it is still function of process and temperature. The sizing of the bias generator is available in Appendix A.

### 4.2.2 Bias Transistor Sizing

The bias transistor  $M_{b5,6}$  and  $M_{b9,10}$  need to be correctly biased as the set quiescent dc voltage for the output transistor M5. From step 5 of the design procedure, the overdrive voltage of the output transistor is known. The overdrive voltage  $V_{eff5}$  is required to be the same on  $M_{b5,6}$  and  $M_{b9,10}$  for setting the appropriate dc quiescent voltage.

$$\left(\frac{W}{L}\right)_{Mb5} = \frac{2I_{db5}}{\mu_n C_{ox} V_{eff5}^2} \quad \text{Equation 4.2}$$

$$\left(\frac{W}{L}\right)_{Mb6} = K \left(\frac{W}{L}\right)_{Mb5} \quad \text{Equation 4.3}$$

$$\left(\frac{W}{L}\right)_{M9,10} = \frac{2I_{db1}}{\mu_n C_{ox} V_{eff5}^2} \quad \text{Equation 4.3}$$

## 4.3 Simulation Results

This section expands on the simulation results obtained from the indirect feedback frequency compensation technique. Figure 4-3 shows the open loop frequency response of the amplifier. The unity gain frequency is at 2.01 MHz, and the corresponding the phase margin is  $61^\circ$ . The amplifier behaves as a two pole system with one non dominant pole. The open loop gain achieved 72 dB. Figure 4-4 depicts the large signal transient response. As the phase margin is ample, there is marginal overshoot and the transient settling is quick as well. The slew rate achieved during charging and discharging are  $1.262\text{V}/\mu\text{s}$  and  $2.44\text{V}/\mu\text{s}$  respectively. Figure 4-5 shows the closed loop response of the amplifier with the different closed loop gains. The summary of the all the specifications are reported in Table 4-4.

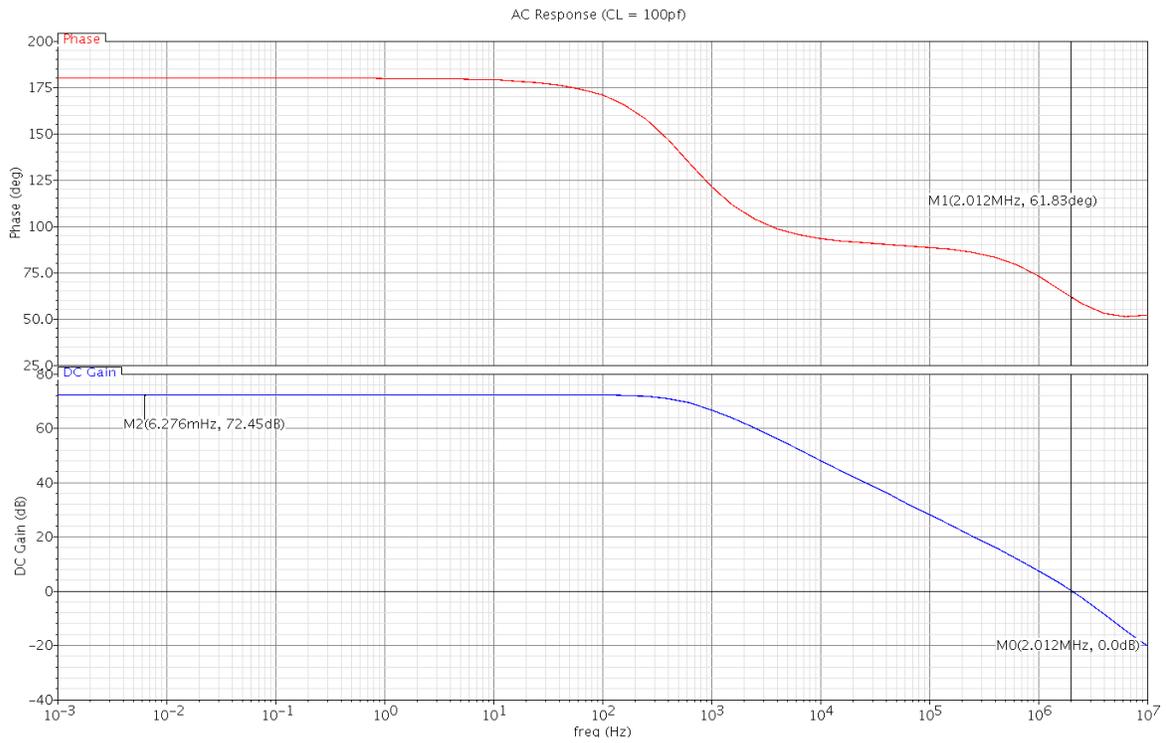


Figure 4-3 AC Frequency Response of Indirect Feedback Compensation Amplifier

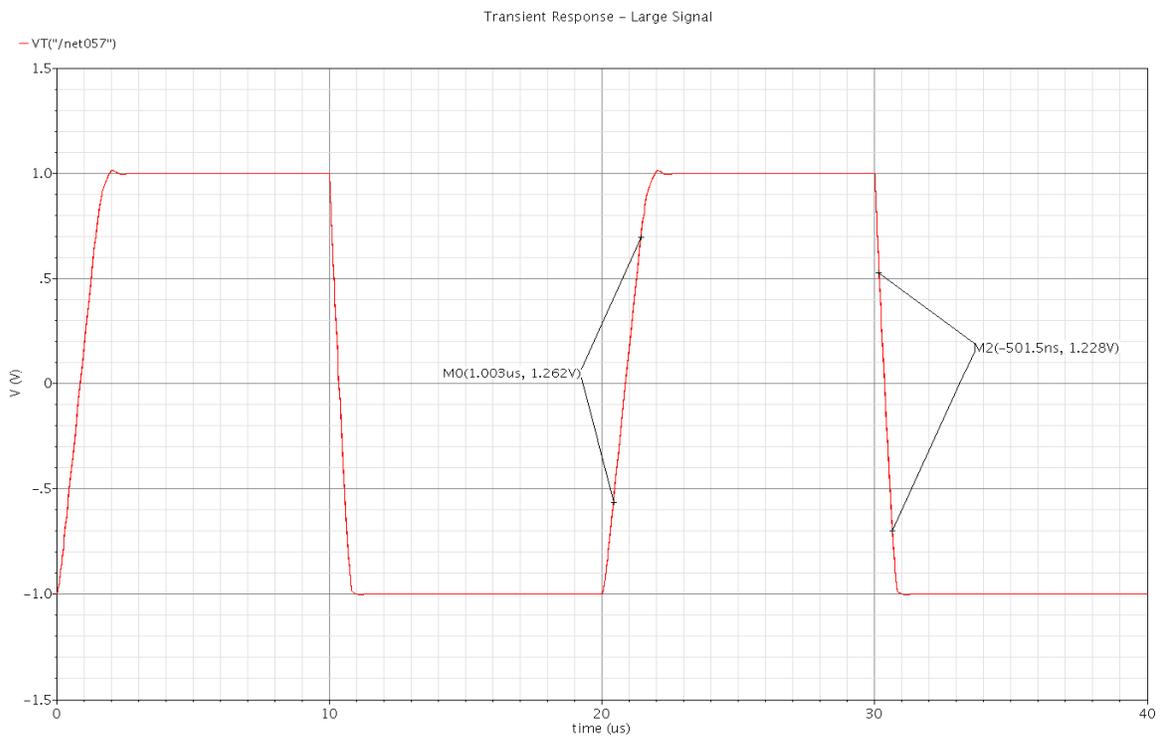
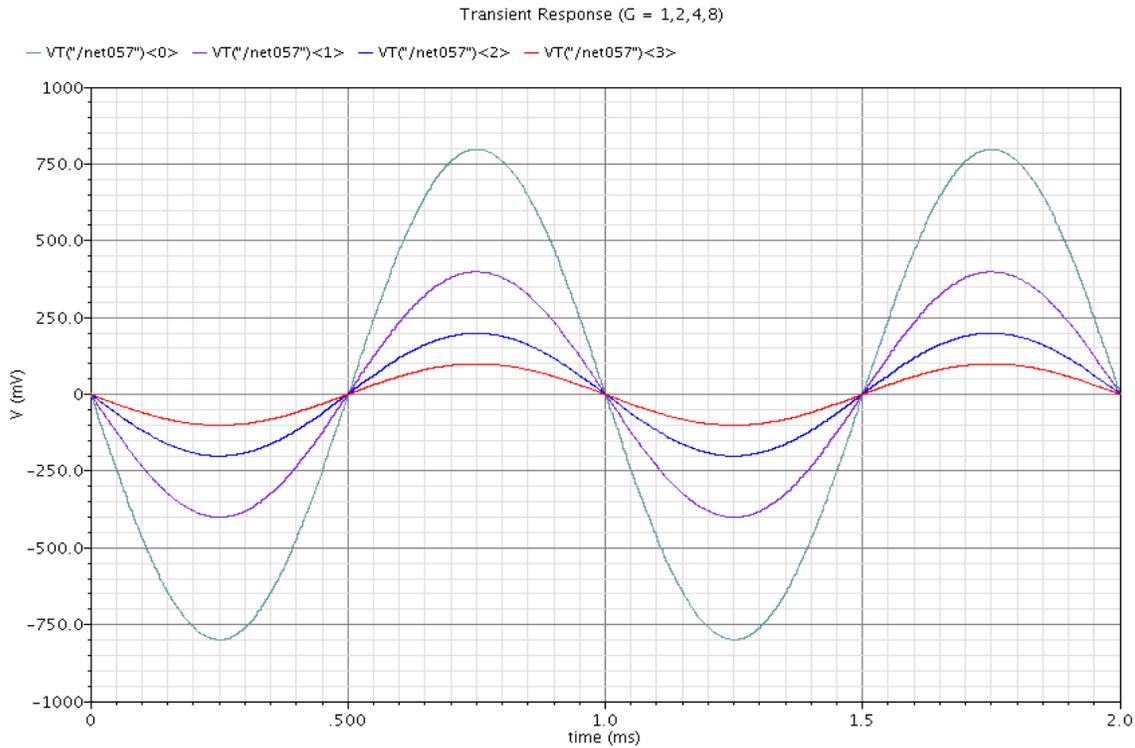


Figure 4-4 Large Signal Transient Response of Indirect Feedback Compensation Amplifier



**Figure 4-5 Closed Loop Transient Response of Indirect Feedback Compensated Amplifier**

**Table 4-4 Simulated Results for Indirect Feedback Compensated Amplifier**

<b>Simulated Results</b>		
Specification	Specifications	Simulation
DC gain: $A_o$	70 dB	72.45 dB
Unity-Gain Frequency: $f_u$	2 MHz	2.01 MHz
Phase Margin: $\phi_M$	$60^\circ$	$61.83^\circ$
Slew Rate: $SR_{+/-}$	$\pm 1$ V/ $\mu$ s	1/-2.45 V/ $\mu$ s
Input Common Mode Range: $V_{CMR+} / V_{CMR-}$	$\pm 0.5$ V	1.1/-0.75 V
Output Swing: $V_{out_{MAX}} / V_{out_{MIN}}$	$\pm 1$ V	1.14/-1.1
$I_{Total}$	-	30 $\mu$ A
Power	-	75 $\mu$ W

The achieved performance of the amplifier meets the required specifications in Table 4-1. However it is still important to verify the mathematical derivation developed in Chapter 3. Table 4-5 lists the relevant transconductance and parasitic values used during calculation and the achieved values during simulation. While Table 4-6 compares the pole locations predicted by Equations 3.20-3.24 and the simulation.

**Table 4-5 Relevant Design Parameters**

Relevant Design Parameters				
Parameter	Equation	Design Procedure	Calculated using Simulation	Simulated
$gm_1$	$gm_{1,2} = \frac{16}{3} \frac{kT}{S_n(f)}$	98 $\mu\text{A/V}$	99 $\mu\text{A/V}$	102 $\mu\text{A/V}$
$C_1$	$C_1 = \frac{2}{3} C_{ox} W_5 L_5$	0.40 pF	0.401 pF	0.401 pF
$C_c$	$C_c = \frac{g_{m1}}{2\pi f_{uf}}$	7.8 pF	5.0 pF	5.0 pF
$gm_5$	$gm_5 = \tan(\varphi_M) \omega_{uf} C_L \frac{C_1}{C_c}$	112 $\mu\text{A/V}$	174 $\mu\text{A/V}$	159.6 $\mu\text{A/V}$
$gm_6(\text{Requirement})$	$gm_6 > 4gm_5 \frac{C_c^2}{C_1 C_L}$	681 $\mu\text{A/V}$	435 $\mu\text{A/V}$	399 $\mu\text{A/V}$
$gm_6$ (Achieved)		-	-	435 $\mu\text{A/V}$

**Table 4-6 Pole and Zero Locations obtained during Simulation**

Comparison of Pole Locations				
Specification	Equation	Calculated using Simulation	Simulated	Percentage Error
$P_1$	$-\frac{1}{g_{m5} R_2 R_1 C_c}$	544 Hz	524.77 Hz	3.66 %
$P_2$	$-\frac{g_{m5} C_c}{C_1 C_L}$	2.218 MHz	2.184 MHz	1.55 %
$Z_1$	$-\frac{g_{mc}}{C_c + C_A}$	11.38 MHz	11.1 MHz	2.52 %
$P_3$	$-\frac{g_{mc}}{\left(\frac{C_c C_L}{C_L + C_c}\right)} + \frac{1}{(R_1    r_{oc}) C_1}$	6.756 MHz	7.771 MHz	13.06 %

From the above two tables it can be confirmed the mathematical insight developed in Chapter 3 agree to the simulation results. The percentage error for the predicted location of the dominant pole and non dominant pole ( $p_1$  and  $p_2$ ) and the left half plane zero are small.

#### 4.4 Alternative Indirect Feedback Compensation Scheme Results

In section 3.3 and 3.4 alternative ways for implementing indirect feedback were presented. Section 3.3 routes the indirect feedback to the low impedance node between the current source and cascode node on the PMOS side. While Section 3.4 has the compensation capacitor connected to the low impedance node between the input pair and cascode node on the NMOS side. The schematics with complete transistor sizing are available in Appendix A. Table 4.7 shows the result achieved from the two architectures and compares it to the indirect feedback to a separate common gate stage amplifier in Figure 4-1.

**Table 4-7 Comparison of Alternative Feedback Compensation**

<b>Comparison of Alternative Indirect Feedback Compensation</b>			
Specification	Common Gate	Cascode NMOS	Cascode PMOS
DC gain: $A_o$	72.45 dB	91.1 dB	86.1 dB
Unity-Gain Frequency: $f_u$	2.01 MHz	1.99 MHz	2.2 MHz
Phase Margin: $\phi_M$	61.83°	61.29°	61.7°

Table 4-7 verifies the alternative architectures achieve the same performance but with a higher gain as the cascode connections increase the output impedance of the amplifier. The cascoded indirect feedback saves area as the common gate amplifier is embedded inside the cascode connection. The cascode compensation thus is a better alternative, however the degree of freedom in choosing the transconductance of the cascode transistor gets limited.

## 4.5 Performance Comparison to Miller Compensation and Single Stage Amplifiers

The proposed amplifier performance is compared to the most standard miller compensation technique. Miller compensation as explained in section 2.4.2 relies on pole splitting method for achieving closed loop stability. The technique thus significantly narrows the bandwidth of the amplifier. As the scheme boosts of bandwidth of extension, it therefore also becomes necessary to compare the performance of the indirect feedback technique to a single stage amplifier employing the same total current and transconductance. Table 4-8 summarizes the comparisons.

**Table 4-8 Comparison to Miller Compensated and Single Stage Amplifiers**

<b>Comparison with Miller Compensation and Single Stage Amplifiers</b>			
Specification	Single Stage	Single Miler Compensation	Indirect Feedback Compensation
DC gain: $A_o$	36.93 dB	70.45 dB	72.45
Unity-Gain Frequency: $f_u$	1.098 MHz	209.1 KHz	2.01 MHz
Phase Margin: $\phi_M$	90°	60.29°	61.7°
$C_c$ Required	-NA-	35 pF	5 pF

Observing Table 4-8 it can be noticed that the indirect feedback compensation outperforms both the single stage architecture and miller compensated amplifiers. In comparison to miller compensation the indirect feedback achieves 10 times higher speed and simultaneously 7 times less area based on the compensation capacitor area. Further the technique even achieves twice the speed in comparison to single stage amplifiers. The increased bandwidth extension is achieved primarily due to the large ratio between the compensation capacitor ( $C_c$ ) and the parasitic capacitor ( $C_1$ ) as observed in equation 3.23. The technique is extremely fruitful for large capacitive loads as the ratio of  $C_c/C_1$  is larger in such cases.

## 4.6 Performance Comparison to Literature

The performance of the proposed three-stage Op Amp topologies is compared with the ones reported in the literature. A set of figure of merits (FoMs) have been defined earlier in section 3.7 to compare various two-stage topologies. Table 4-9 presents a comprehensive comparison of the two-stage Op Amp topologies reported in literature using FoM's described earlier. As it can be seen in Table 4-8, the indirect compensated two stage Op Amps outperform all other Op Amps reported in literature in gain bandwidth metric IFOM<sub>s</sub>. These Op Amps also exhibit much higher slew rate metric than most of the other amplifiers. One can also observe that the proposed Op Amps have been designed with much lower power consumption when compared to the reported Op Amp in Table 4-9, and yet achieve the highest speeds and fast large signal transient response. The proposed procedure thus reveals the true potential of the two stage amplifiers.

**Table 4-9 Comparison of Two Stage Op Amp Topologies**

Conference	Author	Total Id (mA)	GBW (MHz)	Slew Rate (V/μs)	Cl (pf)	IFOMs (MHz•pf)/mA	IFOM <sub>L</sub> ((V/μs)•pf)/mA
ECCTD -2007 [25]	Pennisi	1.950	700.00	2000.00	0.3	107.69	307.69
TCAS - 2005 [24]	Mahattanakul	0.076	5.00	6.00	5	330.69	396.83
WESEAS -2006 [26]	Franz	12.800	1060.00	863.00	4	331.25	269.69
JCSC 2008 [27]	Hamed	7.667	300.00	-NA-	8.5	332.61	-NA-
JSSC - 1995 [28]	Kovacs	0.110	4.50	-NA-	10	409.09	-NA-
AICSP - 2009 [29]	Pugliese	0.318	27.10	25.00	10	851.71	785.71
TCAS - 1997 [6]	Palumbo	0.158	28.00	6.59	5	886.08	208.54
E-Letter 2007 [30]	Pugliese	0.032	6.70	1.00	10	2125.96	317.31
ECCTD - 2005 [31]	Loikkanen	0.210	6.80	6.40	200	6476.19	6095.24
TCAS - 2008 [18]	Palumbo	0.150	9.89	-NA-	100	6593.33	-NA-
<b>This Work - Cascode NMOS</b>	<b>Kumar</b>	<b>0.025</b>	<b>1.99</b>	<b>1.50</b>	<b>100</b>	<b>7960.00</b>	<b>6000.00</b>
<b>This Work - Common Gate</b>	<b>Kumar</b>	<b>0.025</b>	<b>2.00</b>	<b>2.00</b>	<b>100</b>	<b>8000.00</b>	<b>8000.00</b>
<b>This Work - Cascode PMOS</b>	<b>Kumar</b>	<b>0.025</b>	<b>2.20</b>	<b>2.00</b>	<b>100</b>	<b>8800.00</b>	<b>8000.00</b>

## 4.7 Layout

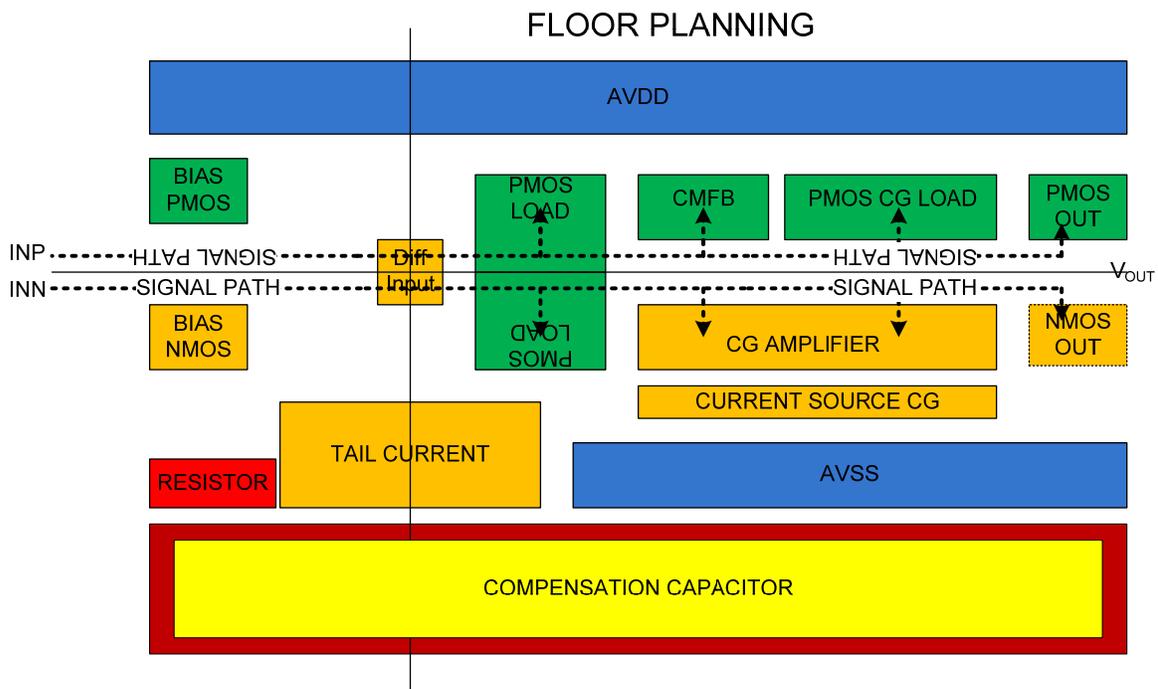
This prototype design of the indirect feedback frequency compensation is implemented in AMI 0.5 $\mu\text{m}$  CMOS process, and will be fabricated through MOSIS research run. In analog design, matching is very important. Particularly, Op Amps need high matching to achieve low input referred offset and high noise rejection. The matching between transistors is mainly dependent on

- Size of transistors
- Shape of transistors
- Orientation of transistors

In general large transistors have more accurate matching than small transistors since the large gate area reduces the impact of localized variation, long channel transistors have better matching than short channel since longer channel alleviate linewidth variation and channel modulation effects. Transistors placed in the same orientation have more precise matching than those in different direction. There in thus design, larger transistors are sized with length of 1 $\mu\text{m}$  and smaller transistors are sized with length 2 $\mu\text{m}$  to obtain larger gate area. Symmetrical layout is necessity for analog mixed signal designs, and thus all stages in this Op Amp are laid out symmetrically. The output source follower and common gate stage consume the most power and thus produce thermal gradients. To avoid unbalanced effects to the input differential pair, they are placed across the thermal line by the weighted power distribution. Power and ground buses are compromised of several metal layers and a wide cross section of buses is chosen to lower resistance and keep the voltage consistent. Dummy segments are placed as required to improve matching.

Floor planning is an essential step before layout as it helps to consider some of the issues mentioned above. Figure 4-6 shows the floor plan for the proposed Op Amp. As seen the transistors are placed across the thermal line to manage thermal gradients generated. The output and common gate transistors consume the highest power, and are thus placed across the thermal line by their weighted power distribution. The signal path runs through the middle of the layout guarded by any noise from the supplies.

The input differential pair is placed on the center of the die and is laid out in a common centroid cross coupled nature to reduce 2<sup>nd</sup> order gradient effects. Wide power buses are placed above and below for easy routing to PMOS and NMOS transistors. Figure 4-7 shows the layout for the amplifier.



**Figure 4-6 Floor planning for two stage amplifier with indirect feedback frequency compensation**

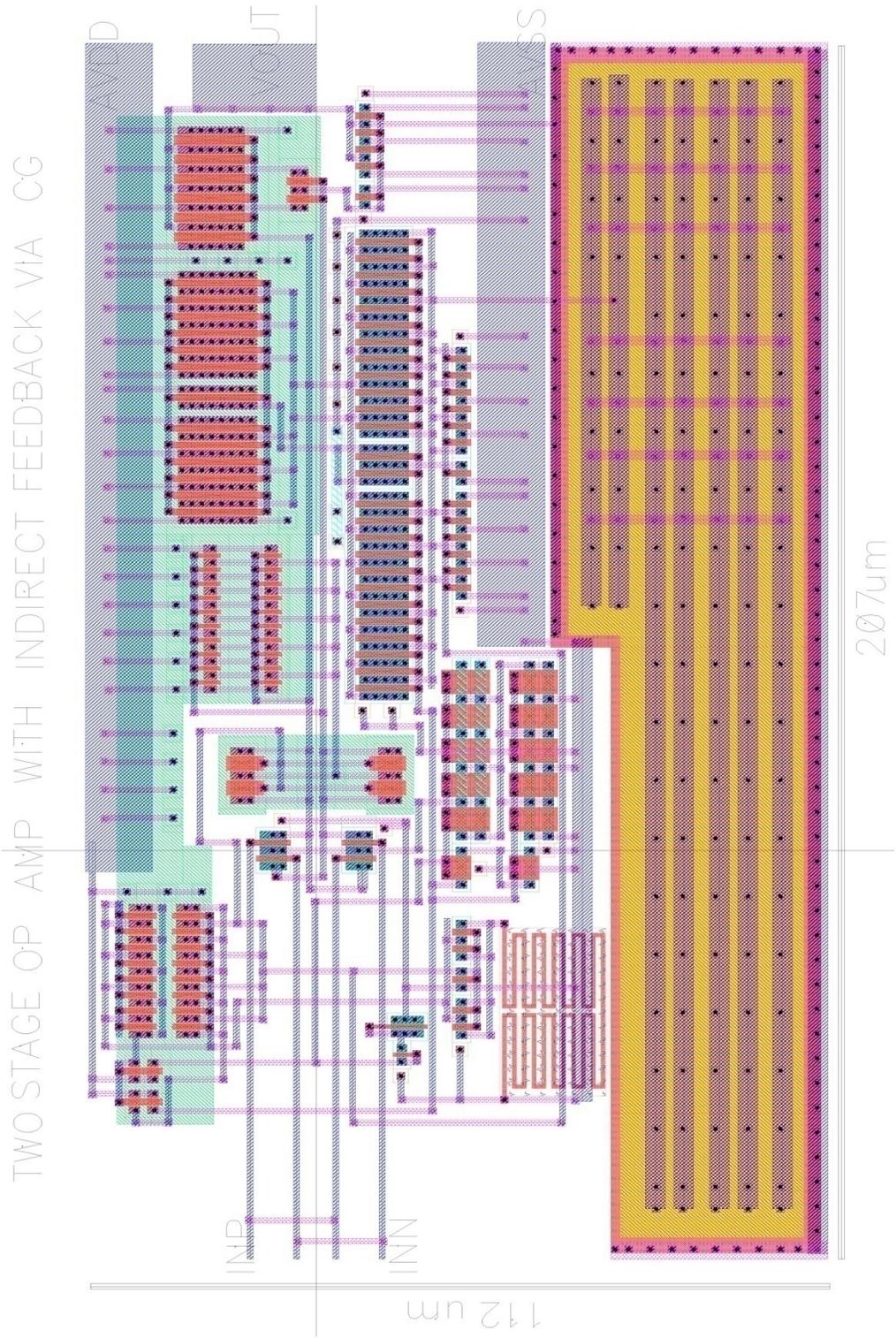


Figure 4-7 Layout of Two Stage Op Amp with Indirect Feedback Compensation

## CHAPTER 5. CONCLUSIONS AND FUTURE WORK

In this thesis, compensation methods for Op Amps are investigated along with their pros and cons in order for a designer to choose the appropriate scheme for a particular application. This thesis further explores a creative indirect feedback compensation method which overcomes the major drawback of bandwidth narrowing by the widely used pole-splitting method. It can improve the phase margin as well as extend the bandwidth of the Op Amp. The indirect feedback method can be easily applied to the existing popular two gain stage Op Amp architectures with very little alteration. The mathematical derivation and circuit simulation demonstrate the advanced properties and improved performance of this feedforward compensation technique.

The indirect feedback technique discussed in this thesis is a practical and superior compensation scheme for Op Amps, and results in amplifiers with much higher speeds and smaller areas. The design procedure proposed in this thesis provides simple step by step instructions in designing such an amplifier. The two stage Op Amp designed as a part of this work achieved extremely high performance in comparison to the state of art research works. The amplifier achieved 2 MHz gain bandwidth product while driving a large 100 pF load while using only 30  $\mu$ A of current. In comparison to the simple miller compensation, the achieved GBW is 10 times larger, and the compensation capacitor is 7 times smaller thus requiring a much smaller area. The Op Amp achieves even two times higher GBW in compared to single stage amplifier with the same total current and total transconductance.

The technique promises great potential in achieving high speed at low power. As a part of future research the compensation method developed for the two stage amplifier can be extended to realize a three stage and multi-stage amplifiers. A formal derivation and design

procedure for multi stage amplifier employing can be developed using the indirect feedback frequency compensation technique.

Indirect feedback frequency compensation technique provides a compatible low voltage, low power Op Amp design which can be used to construct high performance data converters, analog filters and other signal processing blocks in the modern sub micron CMOS process. The technique presented in this thesis should facilitate the integration of analog circuits in the modern low power high speed applications.

## APPENDIX A. Schematics

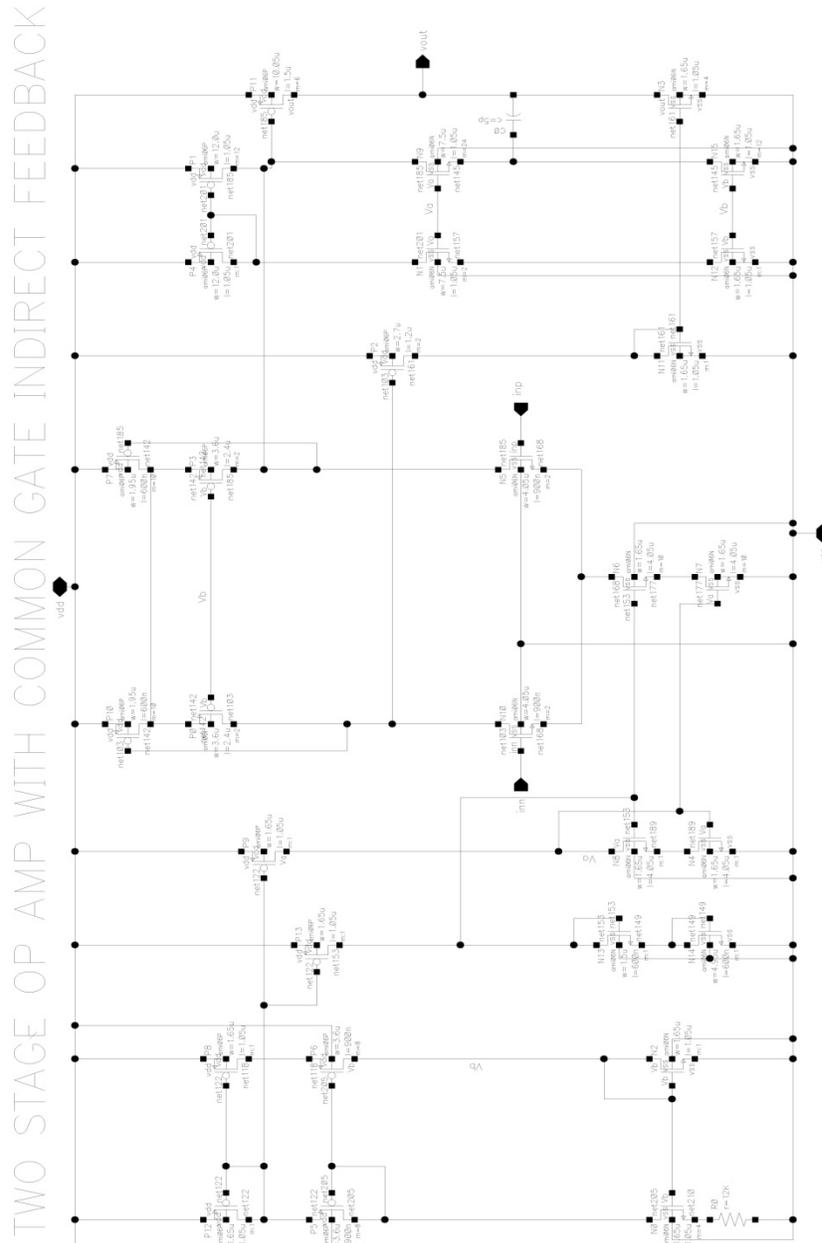


Figure 5-1 Two Stage Op Amp with Common Gate Indirect Feedback Frequency Compensation

TWO STAGE OP AMP WITH INDIRECT FEEDBACK TO PMOS CASCODE NODE

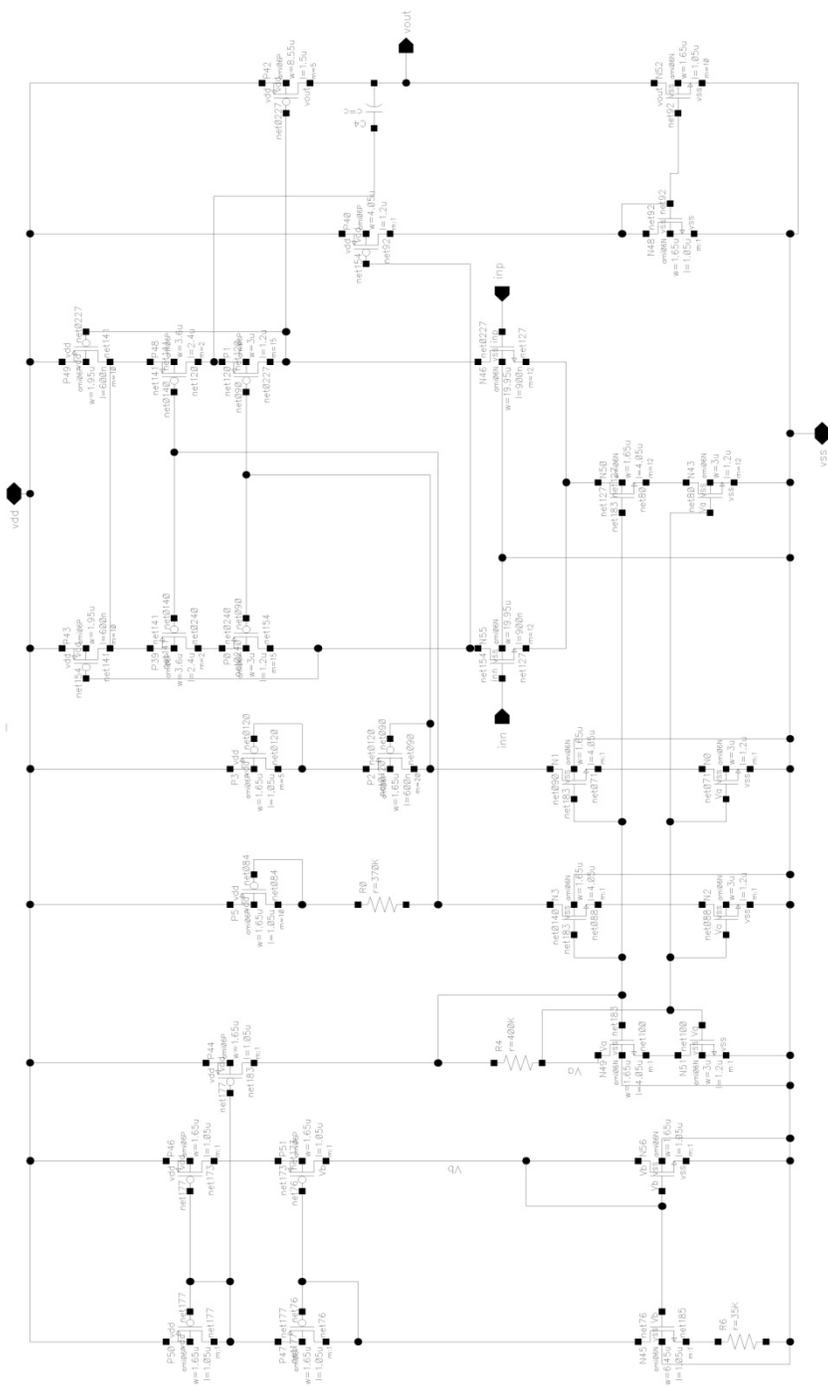


Figure 5-2 Two Stage Op Amp with Indirect Feedback Frequency Compensation to PMOS cascode node



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